FUJI SWITCHINGPOWER SUPPLYCONTROL IC

C-MOS CURRENT MODE CONTROL IC

FA13842／43／44／45

Application Note

Fuji Electric Co.,Ltd.
Matsumoto Factory
February-'98 a

CONTENTS

1. Description

The FA1384X series are CMOS type current mode control ICs for off-line and dc-to-dc converter.

These ICs can reduce start-up circuits loss and are optimum for high efficiency power supply because of low power dissipation of these ICs achieved by CMOS process .

These ICs are can drive a power MOSFET directly.

A high-performance power supply can be designed compactly with minimal external components .

2. Features

- Low-power dissipation by CMOS Process
- Stand-by current 2μA(max.) , start-up current ３０μＡ(max.)
- Pulse-by-pulse current limiting
- 5V bandgap reference
- UVLO with hysteresis
- Maximum duty cycle ９６% (FA13842/43) , ４８% (FA13844/45)
- Pin-for-pin compatible with UC384X

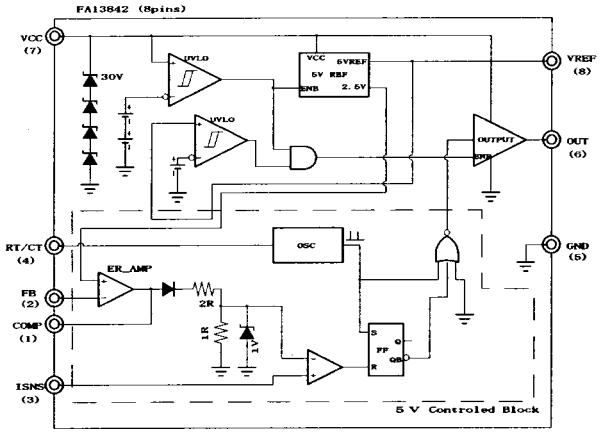
(notice)Pins are compatible, but the characteristics are not fully compatible .
When you applies our ICs to power supply circuit designed for other manufacture's 384X series, you must check the characteristics and the safety on your power supply.

3. Fuji FA1384X series

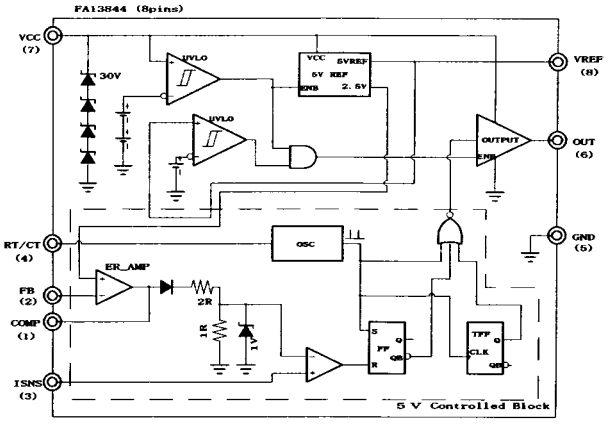
Type name	UVLO		Maximum duty cycle
	Start Threshold	Stop Threshold	
ＦＡ１３８４２Ｐ／Ｎ	１６．５Ｖ±１Ｖ	９Ｖ±１Ｖ	９６%
ＦＡ１３８４３Ｐ／Ｎ	９．６Ｖ±１Ｖ	９Ｖ±１Ｖ	９６%
ＦＡ１３８４４Ｐ／Ｎ	１６．５Ｖ±１Ｖ	９Ｖ±１Ｖ	４８%
ＦＡ１３８４５Ｐ／Ｎ	９．６Ｖ±１Ｖ	９Ｖ±１Ｖ	４８%

※ＦＡ１３８４Ｘ Ｐ：ＤＩＰ package
ＦＡ１３８４Ｘ Ｎ：ＳＯＰ package

4. Block diagram



FA13842/43



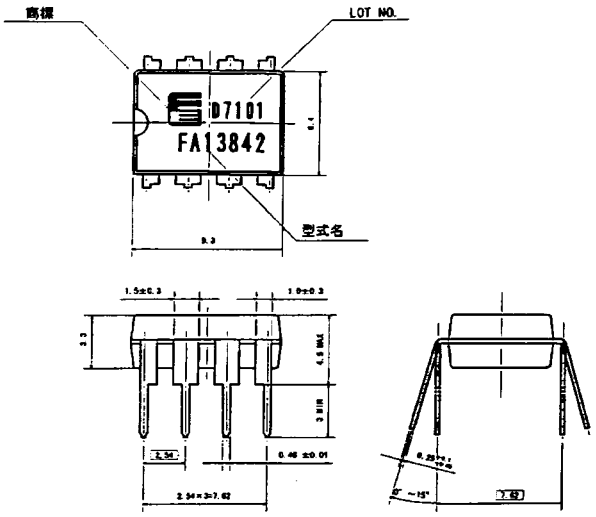
FA13844/45

・Pin description

Pin No.	Symbol	Function	Description
1	COMP	Compensating	Error amplifier output, available for loop compensation circuit
2	FB	Feedback	Inverting input of the error amplifier
3	ISENS	Current sense	Input voltage proportional to inductor current
4	RT/CT	Oscillator control	Setting oscillation frequency and maximum duty-cycle by resistor Rt and capacitor Ct
5	GND	Ground	Ground
6	OUT	Output	Output for driving a power MOS-FET
7	VCC	Power supply	Power supply
8	VREF	Reference voltage	Reference voltage and current source charging capacitor CT through resistor RT

5. Outline diagram

DIP



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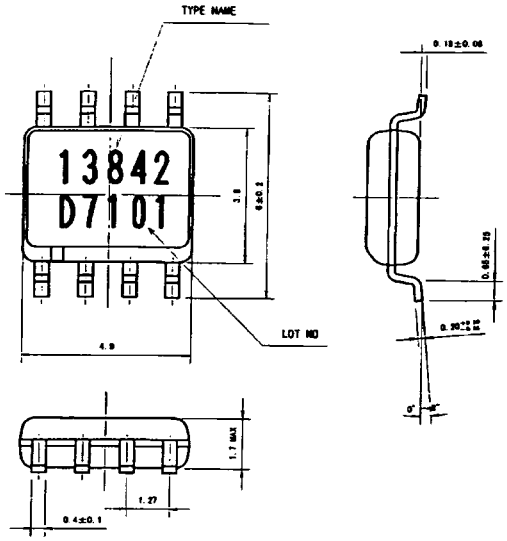

6. Ratings and Electrical characteristics

6－1. Absolute maximum ratings

Item	Test condition		Rating	Unit
Supply voltage	Low impedance source		28	V
	Zener clamp (Icc<10mA)		self Limiting	V
Zener current			10	mA
Output peak current	source current		400	mA
	sink current		1	A
FB/ISNS terminal input voltage	FB, ISNS		-0.3～5.3	V
Error amplifier sink current			10	mA
Total power dissipation	at Ta <50℃	DIP	800	mW
		SOP	400	
Thermal resistance θj-a	junction－air	DIP	125	℃/W
		SOP	250	
Junction temperature			150	℃
Ambient temperature			-25～85	℃
Storage temperature			-40～150	℃

6－2. Recommended operating conditions

Item	MIN	MAX	Unit
Supply voltage	10	25	V
Oscillation timing resistor	2.0	100	kΩ
Oscillation timing capacitor	0.47	10	nF
Oscillation frequency	10	500	kHz

6－3. Electrical characteristics (Vcc=15V, RT=10k, CT=3.3nF, Ta=25℃)

1. Reference voltage section						
Item		Test condition	Min.	Typ.	Max.	Unit
Reference voltage		Tj=25℃, IL=1mA	4.75	5.00	5.25	V
	Line regulation	Vcc=10～25V		±3	±20	mV
	Load current regulation	IL=0～20mA		±3	±25	mV
	Temperature regulation	Ta=-25～85℃		±0.3		mV/℃
Output current at short-circuit		Tj=25℃		60		mA

2. Oscillator section						
Item		Test condition	Min.	Typ.	Max.	Unit
Oscillation frequency		Tj=25℃ Ta=-25～85℃	49 47	52	55 57	kHz
	Voltage stability	Vcc=10～25V		±0.25	±1	%
	Temperature stability	Ta=-25～85℃		-0.07		%/℃
Oscillation amplitude		Tj=25℃		1.6		V
Discharge current		Tj=25℃		8.4		mA

.Error amplifier section					
Item	Test condition	Min.	Typ.	Max.	Unit
Input voltage	COMP=2.5V, Tj=25℃	2.4	2.5	2.6	V
Input leak current				±2	μA
Open-loop gain		65	72		dB
Unity gain bandwidth		0.7	1		MHz
Output source current	FB=2.3V, COMP=0V	-0.8	-1.0		mA
Output sink current	FB=2.7V, COMP=1V	2	15		mA
Output voltage	FB=2.3V RL=15k to GND	4.0	4.5		V
	FB=2.7V RL=15k to VREF		80	500	mV

4. Current sense section					
Item	Test condition	Min.	Typ.	Max.	Unit
Voltage gain	Tj=25℃	2.85	3	3.15	V/V
Maximum input signal	FB=0V	0.9	1.0	1.1	V
Input bias current			-1	-5	μA
Delay to output	Tj=25℃, ISNS→OUT		150	300	ns

5. Output section					
Item	Test condition	Min.	Typ.	Max.	Unit
Output high level	Isource=-20mA	14.5	14.75		V
	Isource=-100	12	13.5		V
Output low level	Isink=20mA		0.15	0.3	V
	Isink=200mA		1.5	3	V
Rise time	CL=1nF, Tj=25℃		40	150	ns
Fall time	CL=1nF, Tj=25℃		20	150	ns

6. Under-voltage lockout section					
Item	Test condition	Min.	Typ.	Max.	Unit
Start threshold	FA13842/44	15.5	16.5	17.5	V
	FA13843/45	8.6	9.6	10.6	V
Min. operating voltage		8	9	10	V
Hysteresis	FA13842/44		7.5		V
	FA13843/45		0.6		V

7. PWM section					
Item	Test condition	Min.	Typ.	Max.	Unit
Maximum duty cycle	FA13842/43	94	96	98	%
	FA13844/45	47	48	50	%
Minimum duty cycle	FB=5V, COMP=open			0	%

8. Total standby current					
Item	Test condition	Min.	Typ.	Max.	Unit
Standby current	Vcc=14V			2	μA
Start-up current	Vcc=start threshold		12	30	μA
Operating current			3	5	mA
Zener Voltage (Vcc)	ICC=5mA	28	30	34	V

7. Characteristics curves

(notice)Common to FA13842/43/44/45 except for Fig. 1, 2, 3, 4, 14

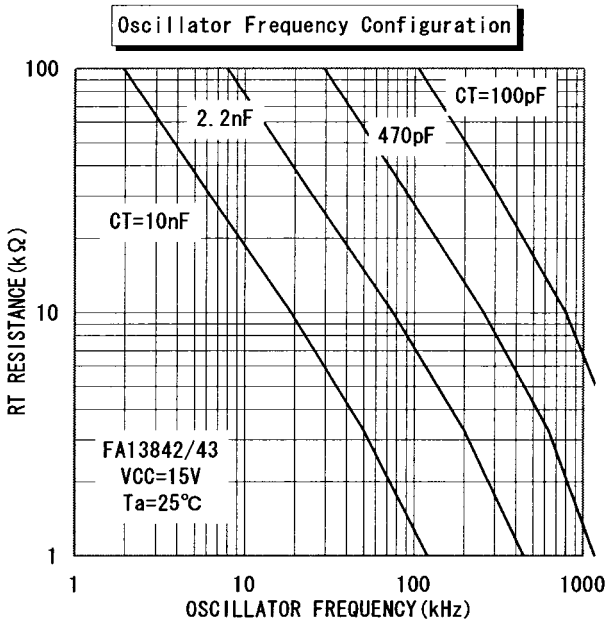

Fig. 1

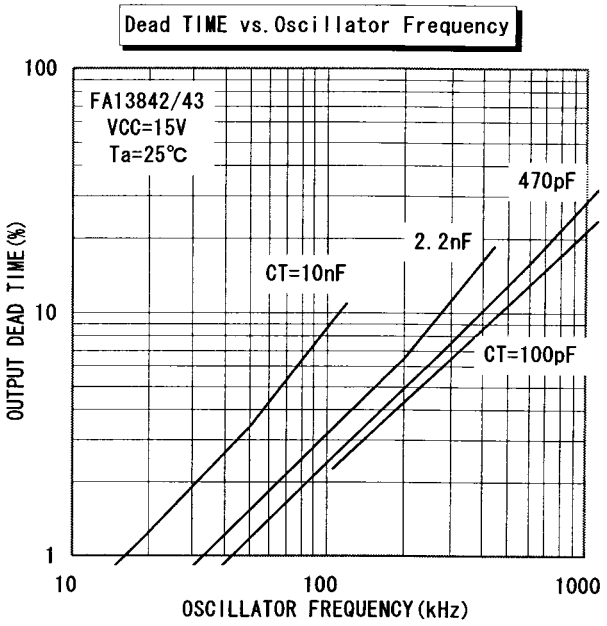

Fig. 2

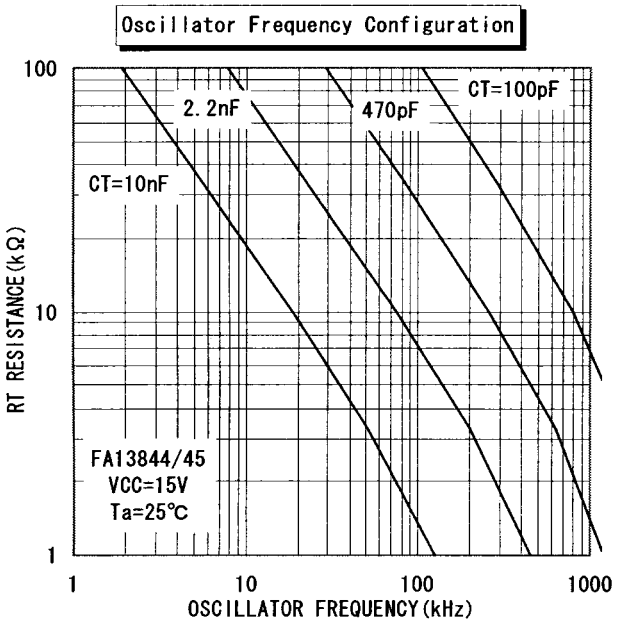

Fig. 3

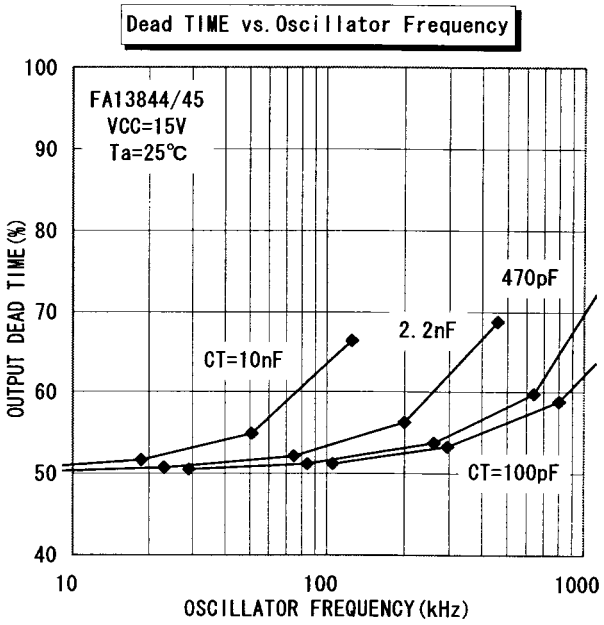

Fig. 4

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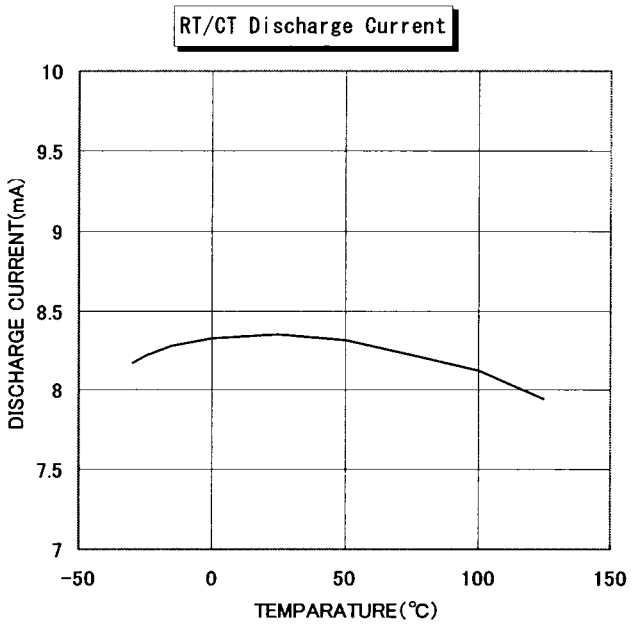

Fig. 5

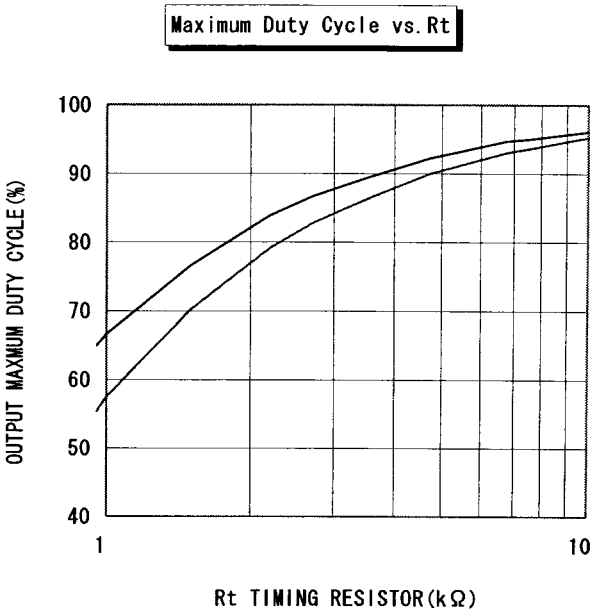

Fig. 6

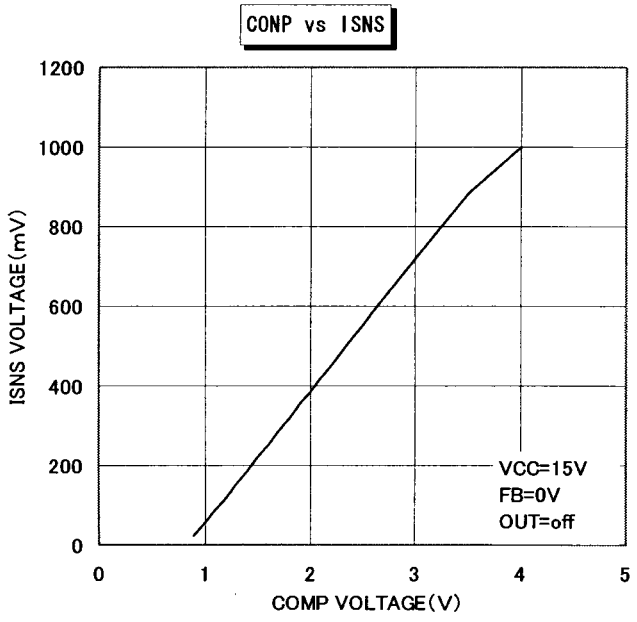

Fig. 7

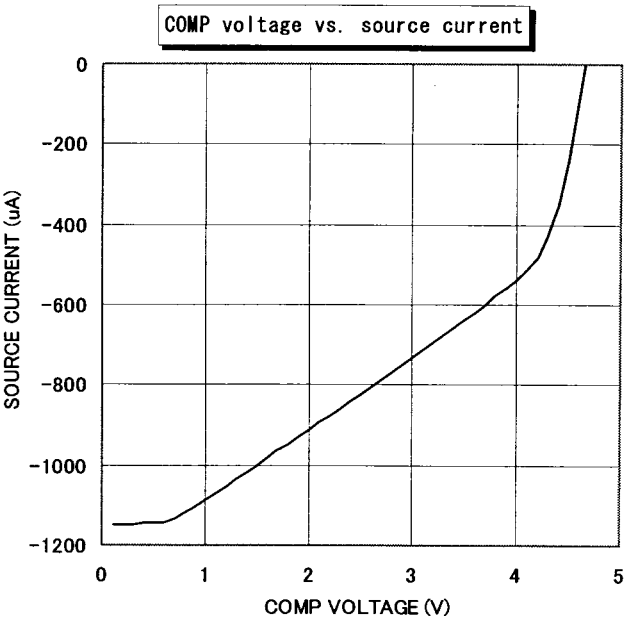

Fig. 8

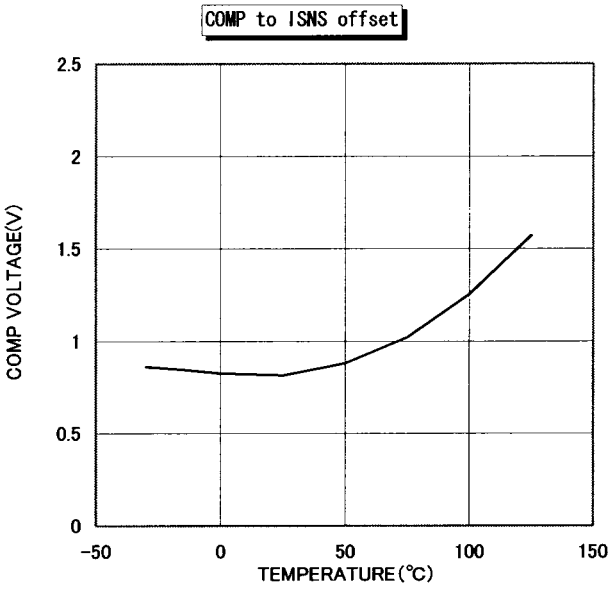

Fig. 9

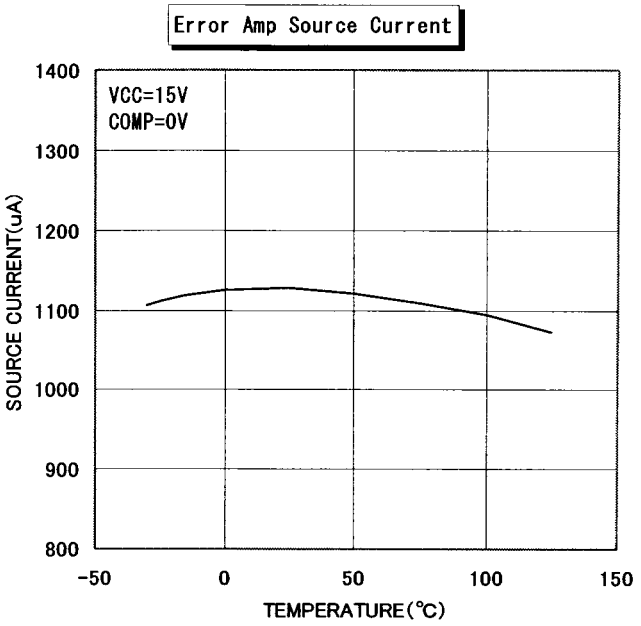

Fig. 10

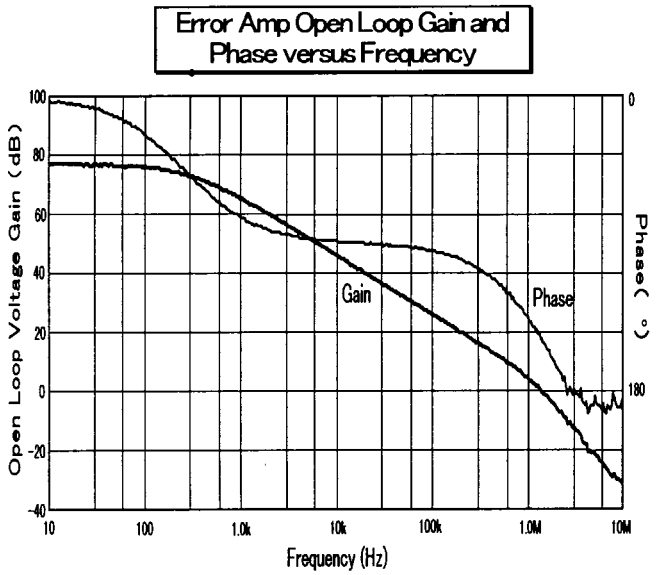

Fig. 11

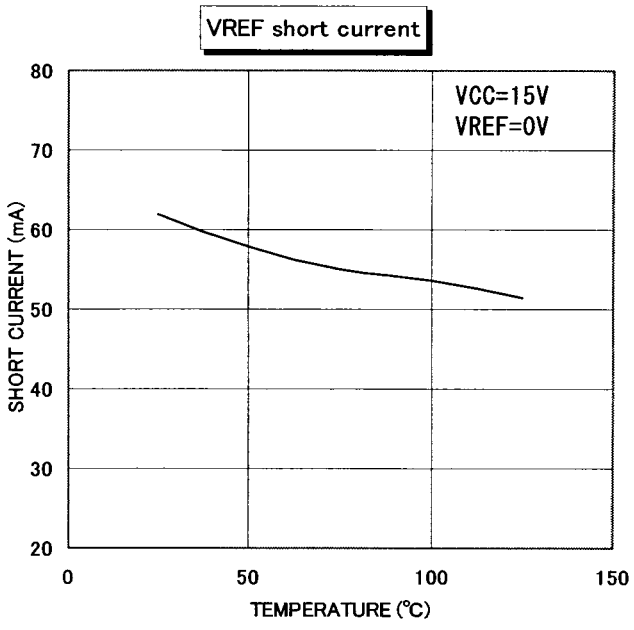

Fig. 12

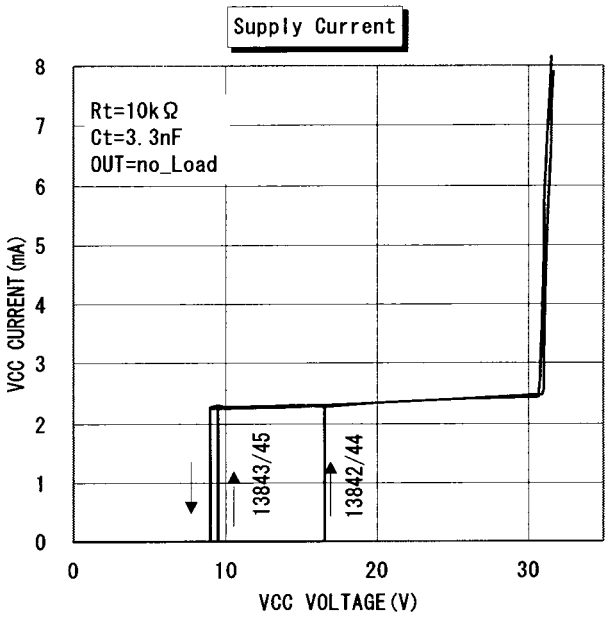

Fig. 13

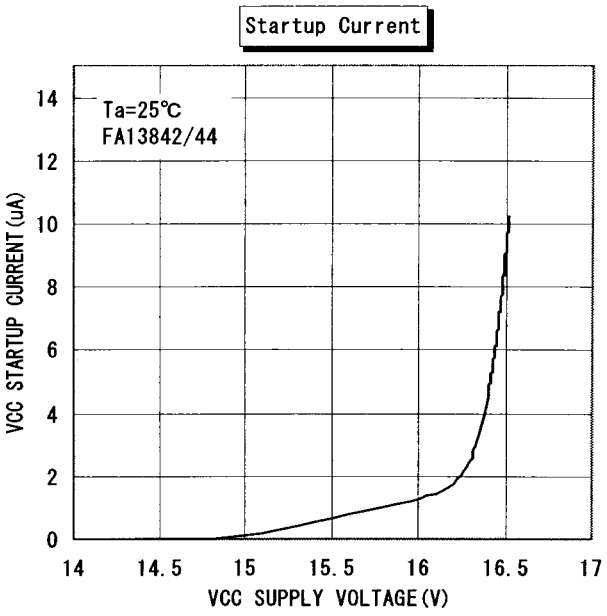

Fig. 14

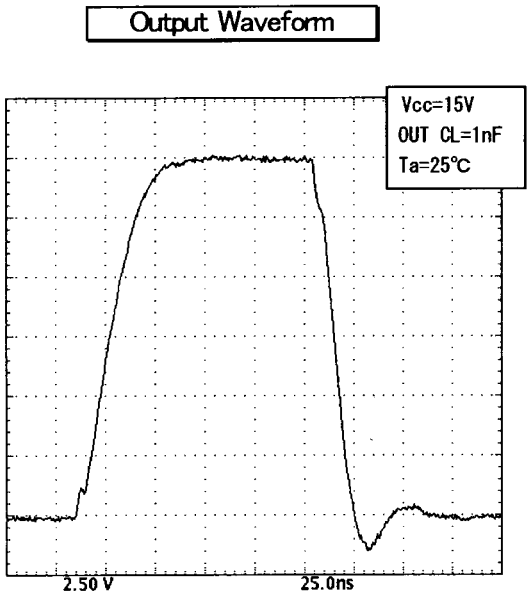

Fig. 15

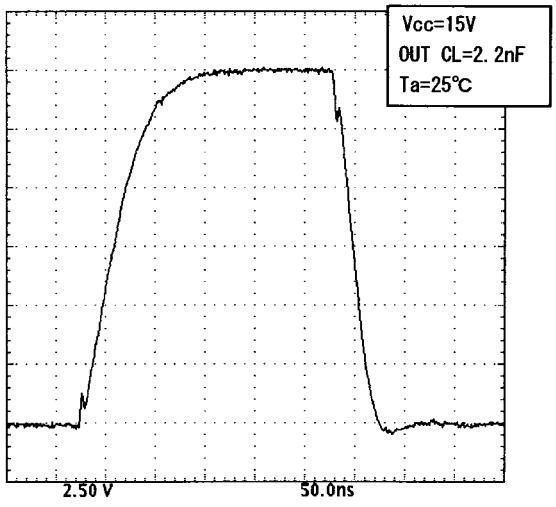

Fig. 16

8. Description of motions of each block

8-1 Oscillator

The oscillation frequency is set by timing resistance Rt and timing capacitor Ct, which are connected to RT/CT terminals. Ct is charged to about 3V through the Rt from the 5V reference , and discharged to about 1.4V by the built-in discharge circuit. (See Fig. 17, 18, 19.)

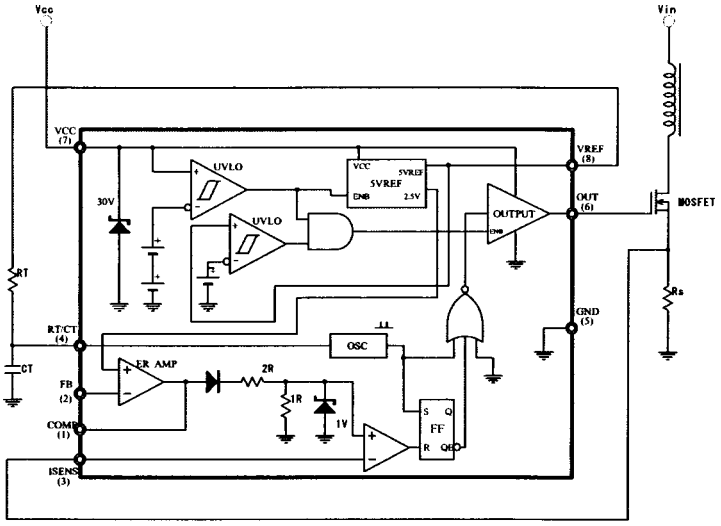

Fig. 17

Blanking pulses are generated in the interior during the Ct discharge period. The output is fixed in the "low" state by these pulses, and a fixed dead time is produced. See the characteristics graphs shown in Fig. 1 - 4 regarding the relation among the oscillation frequency, RT and CT.

In the case of FA13844/45, a flip-flop is contained, and the output is blanked with every other cycle by this flip-flop. Therefore, the switching frequency of a power MOSFET is 1/2 of the oscillator frequency set by Rt and Ct. (See Fig. 19.)

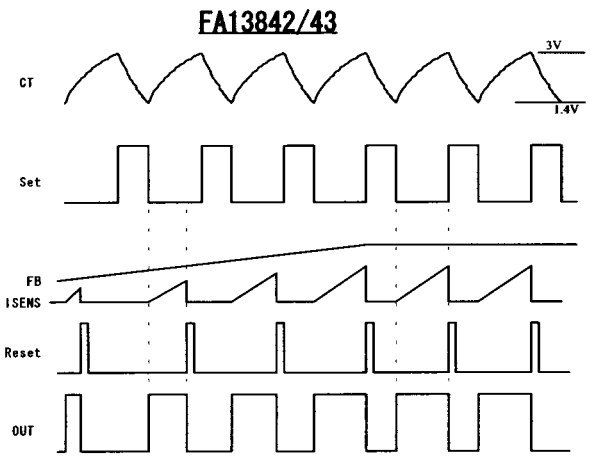

Fig. 18

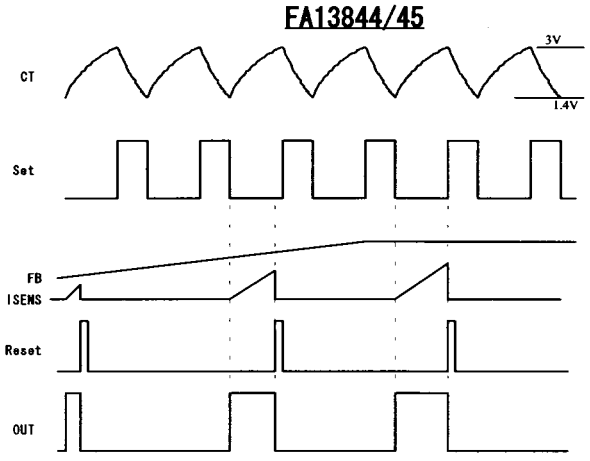

Fig. 19

8-2 Error amplifier

Inverting input and output are connected to the FB terminal and COMP terminal respectively. The 2.5V reference is connected internally to the non-inverting input.

The output voltage is offset by diode VF voltage (=0.7V), and divided by three. The divided voltage is connected to the input of the current sense comparator.

8-3 Current sense comparator and PWM latch

"High" state of OUT terminal begins on the starting time of charging Ct. The state of out terminal turns to "Off" when the peak inductor current reaches the threshold level controlled by the error amplifier output (COMP terminal) .

The inductor current is converted to a voltage by sense resistor RS inserted between GND and the source of a power MOSFET. This voltage is monitored by ISNS terminal.

The peak current of inductor "Ipk" is expressed as follows.

$Ipk=(Vcomp-0.7)/(3*Rs)$ $0.7 \fallingdotseq V_F$

Vcomp : a voltage on comp terminal

The maximum value of the threshold level of the current sense comparator is internally clamped at 1V, therefore the maximum peak current "Ipk(max)" is as follows.

$Ipk(max)=1.0V/Rs$

8-4 Under-voltage lockout (UVLO)

In order to set the IC in the complete operation mode before the output stage(OUT terminal) is enabled, two under-voltage lockout comparators are incorporated to monitor the power supply voltage (Vcc) and reference voltage (VREF).

The threshold level of the Vcc comparator is set at 16.5V/9V for FA13842/44 and at 9.6V/9V for FA13843/45. In the standby mode which the Vcc is under ON threshold, the power supply current is kept at nearly 0 (zero). However, a current of 30μA at maximum is required to transfer from standby mode to operating mode .

The threshold level of the VREF comparator is set at about 3.2V/2.0V.

A 30V zener diode is connected Vcc and GND, to protect the IC against overvoltage .

8-5 Output stage

An output stage of CMOS inverter composition is incorporated, and it is possible to fully swing the gate voltage of a power MOSFET to the Vcc.

The output stage provides the capacity of 400mA source current and 1A sink current as the peak current. (When Vcc is 15V)

The output stage is held in the "Low" state at standby mode.

8-6 Reference voltage

The 5.0V(±5%) bandgap reference(Tj=25℃) is built-in.

It is possible to supply current of about 10mA to an external circuit in addition to charge current to the timing capacitor of the oscillator. (See Fig. 12.)

Connect a ceramic bypass capacitor of 0.1μF or higher to the VREF terminal to stabilize this voltage.

9. Advice in the design

9-1 Start-up circuit

A typical start-up circuit is shown in Fig. 20.

The AC INPUT voltage charges capacitor C2 and supply start-up current to the IC through start-up resistance R1. When this voltage reaches the ON threshold voltage, the IC turn to the operation mode and electric power is supplied from the bias winding of the transformer thereafter.

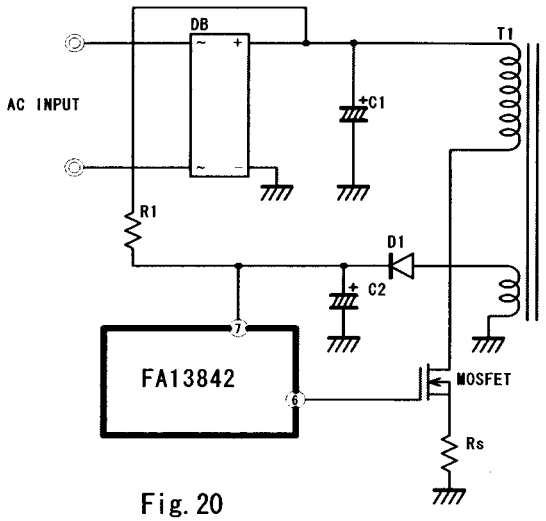

Fig. 20

By means of CMOS process, the start-up current is less than 30μA.

When the start-up resistance is increased, charging of capacitor C2 becomes slower and the start-up time increases. Select the optimum values of R1 and C2 for your circuit.

The relation between the start-up resistance and start-up time for the circuit indicated in Fig. 20 is shown in Fig. 21.

Fig. 22 indicates a method to increase the start-up resistance for reducing its loss and to shorten the start-up time. The start-up time is shortened by reducing the capacitance of C2 and the bias current is supplied from C3 after start-up.

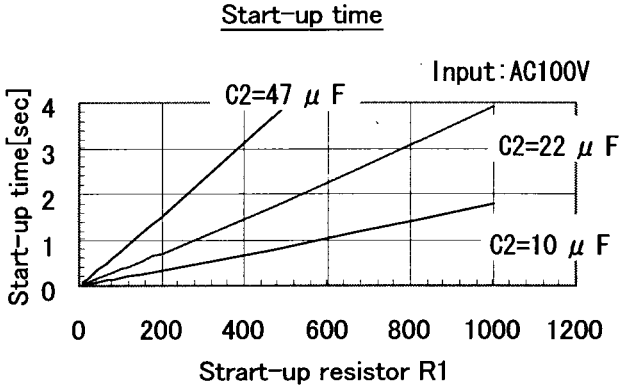

Fig. 21

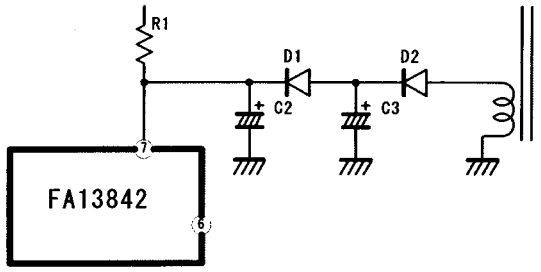

Fig. 22

9-2 Synchronized operation with external signals

Synchronized operation with external signals is permitted with the circuit that is shown in Fig. 23.

Synchronized operation is started when the RT/CT terminal is raised to about 3V or higher. (Synchronized at leading edge.)

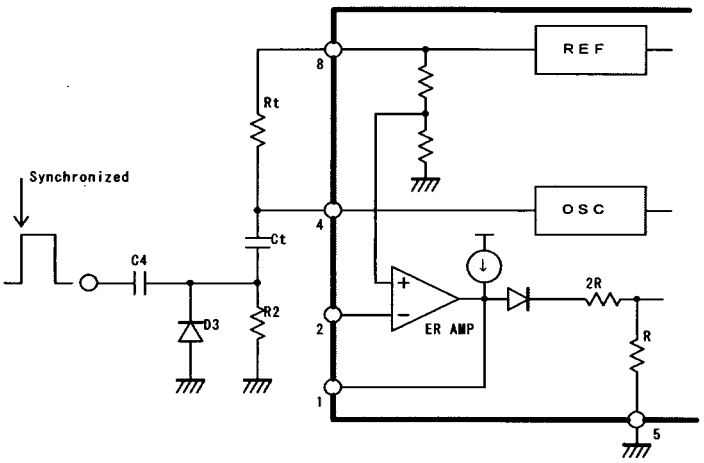

Fig. 23

It is necessary that the external synchronizing signal should be higher than the free run frequency.

In the case of FA13844/45, the output frequency of OUT terminal is 1/2 of the synchronizing signal frequency.

9-3 Latched shutdown

A typical circuit for latched shutdown is shown in Fig. 24.

The voltage of OUT terminal is kept at low state if the voltage of COMP terminal is held at low level. It is necessary that the voltage level of the COMP terminal is set at 0.7V or less in the applied temperature range. (See Fig. 9.)

The source current from COMP terminal is less than about 1.3mA.

Use of such a thyristor shown in Fig. 25 is not effective because the saturation voltage of thyristor is higher than 0.7. When a thyristor is used, pull up the voltage of FB terminal to over 3V as shown in Fig. 26. In the case of latched shutdown , it is necessary to supply current higher than the hold current of the thyristor composing circuit or of the thyristor. This current should be supply through a start-up resistor from AC input.

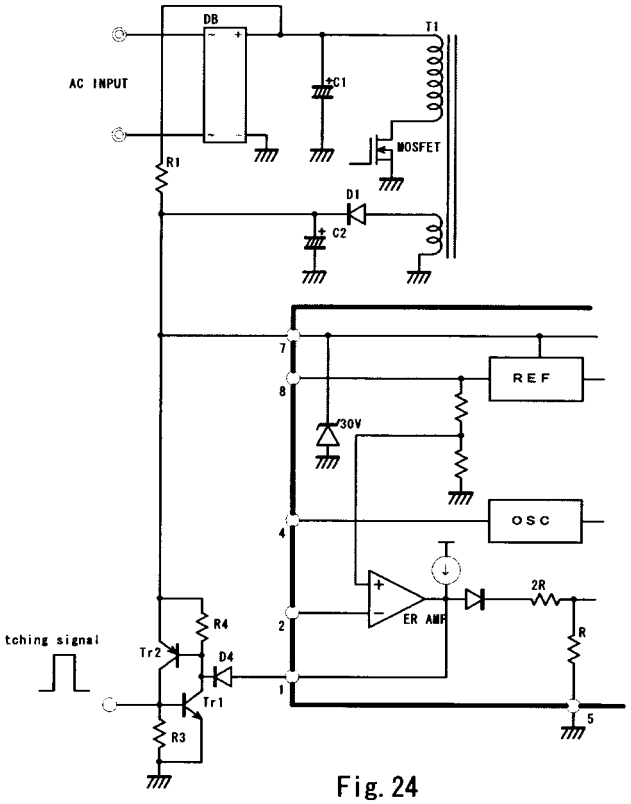

Fig. 24

Latched shutdown by a thyristor using COMP terminal is not effective.

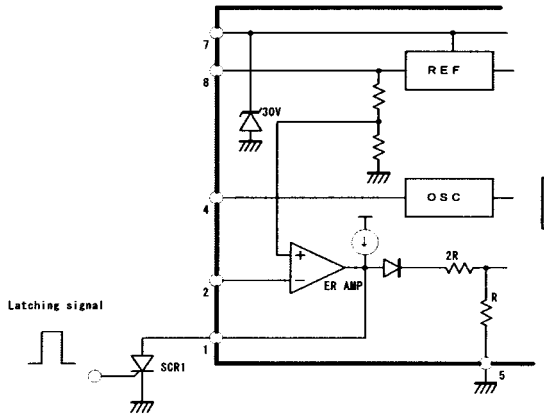

Fig. 25

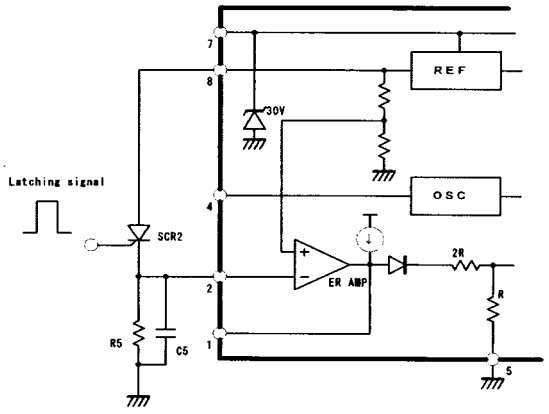

Fig. 26

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① The method for detection of overvoltage (detection on primary side)

A typical circuit of latched shutdown to protect against the overvoltage detected on the primary side is shown in Fig. 27.

When the secondary voltage rises in the flyback circuit, the voltage of the bias winding also rises in proportion to it. When this rise voltage is detected by zener diode ZD1, the latched shutdown is accomplished. Because the secondary voltage is detected through a transformer, the detection accuracy is not high.

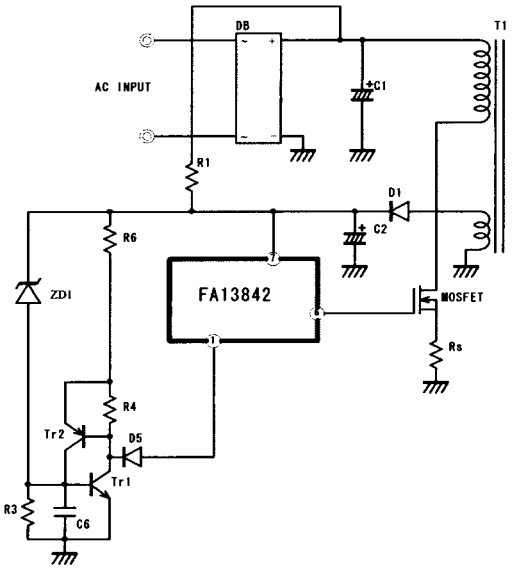


Fig. 27

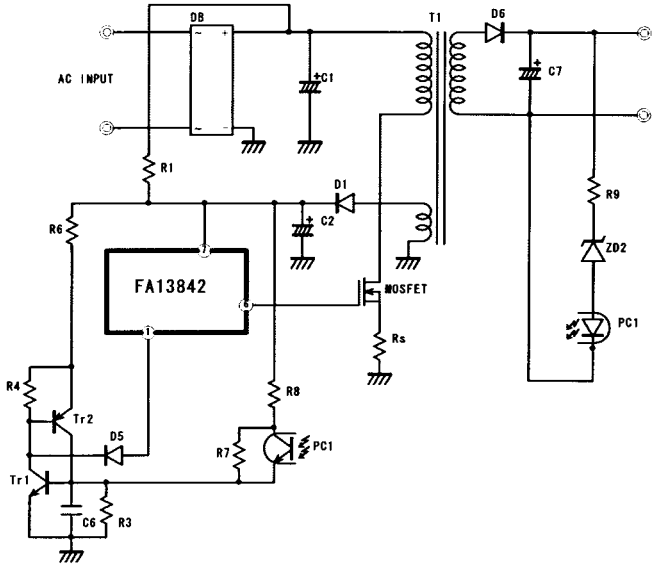


Fig. 28

② The method for detection of overvoltage (detection on secondary side)

A typical circuit of latched shutdown to protect against the overvoltage detected on the secondary side is shown in Fig. 28.

The accuracy of the detected voltage is high compared to detection of overvoltage on the primary side.

③ The method for detection of overcurrent (detection of primary current)

A typical primary overcurrent detection circuit is shown in Fig. 29.

④ The method for detection of overcurrent (detection of secondary current)

A typical secondary overcurrent detection circuit is shown in Fig. 30.

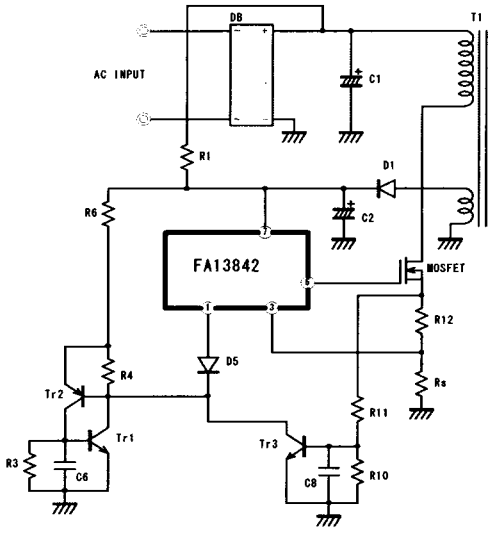


Fig. 29

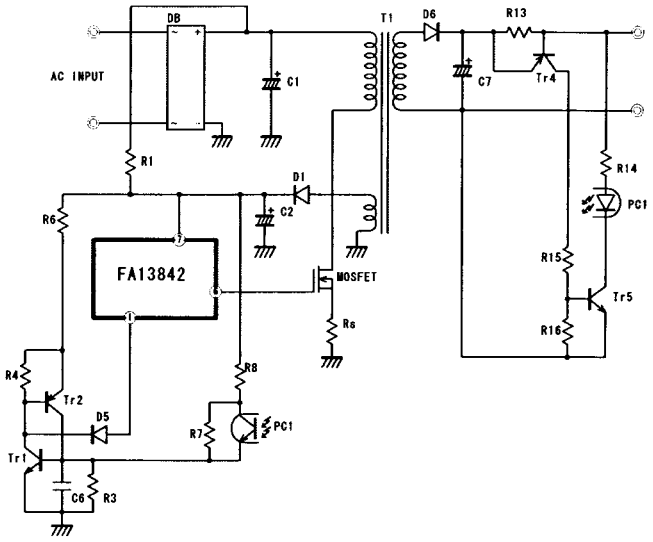


Fig. 30

9-4 Soft start

A soft start circuit is shown in Fig. 31.

The soft start time is determined approximately following equation as the time that a voltage threshold of ISNS terminal reaches.

$$t_{soft\text{-}start}[ms] = 4.3 * C9[\mu F]$$

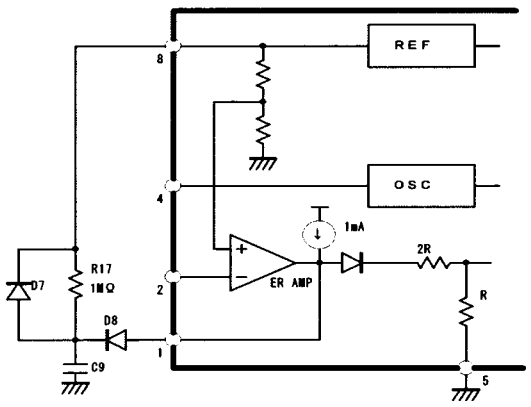


Fig. 31

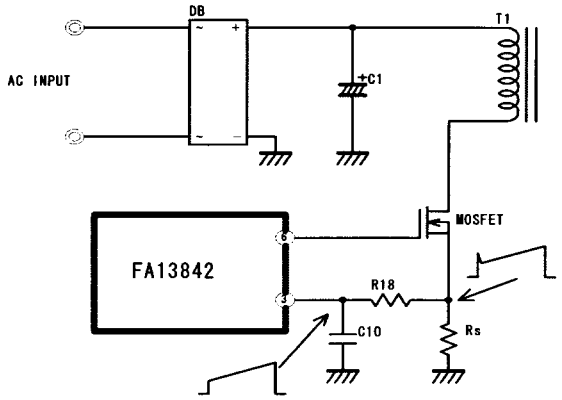


Fig. 32

9-5 Suppression of noise at current sense terminal

Each cycle current value is monitored in current mode control. Therefore, there is a possibility where malfunction occurs even with relatively small noise. It is necessary to add a CR filter to reduce noise at the current sense terminal. (See Fig. 32)

9-6 ON/OFF circuit with an external signal

A typical ON/OFF circuit is shown in Fig. 33.

Output stage (OUT terminal) is enabled when the voltage at FB terminal is reduced to under 2.0V, and Output stage (OUT terminal) is disabled when it rises over 3V.

Set the voltage of FB terminal at 5.3V at maximum in this case.

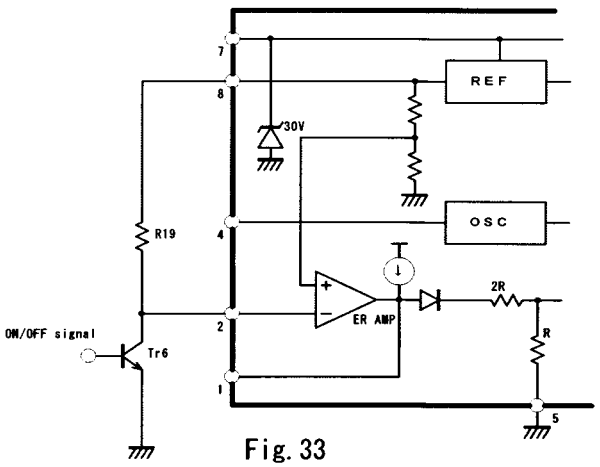


Fig. 33

Fig. 33

9-7 Feedback circuit

(1) The method not using an internal ER AMP

The method not using an internal ER AMP is shown in Fig. 34. Connect FB terminal to GND and connect a optocoupler to COMP terminal of ER AMP output, for feedback control.

It is possible to obtain precise output voltage of power supply ,because the output voltage is monitored directly on secondary side .

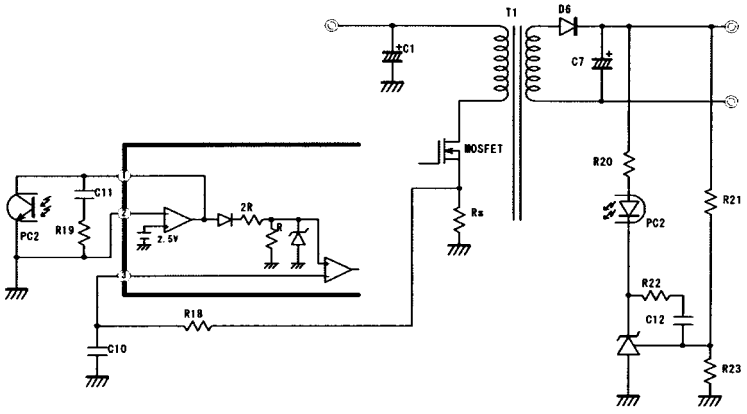


Fig. 34

Be sure to connect FB terminal to GND in this case.
There is a possibility that malfunction occurs if FB terminal is opened.

(2) The method using an internal ER AMP

The method using an internal ER AMP is shown in Fig. 35.

In the flyback circuit, the bias winding voltages of transformer is proportional to the secondary winding voltage. Therefore, Vcc is approximately proportional to the DC output voltage on secondary side.

Vcc is divided by resistor and monitored at FB terminal to control the output voltage.

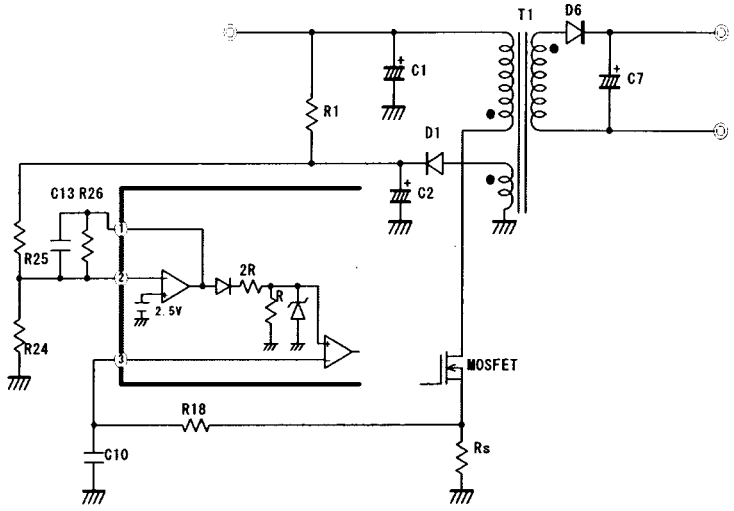


Fig. 35

This feedback circuit consists of minimal external components. However the regulation of the DC output voltage is not good because the output voltage is not directly monitored.

9-7 Slope compensation

It is well known that a current mode converter which controls peak current can oscillate irregularly when inductor current is continuous and a duty cycle is over 50%.
This irregular oscillation is called subharmonic oscillation.
The period of subharmonic oscillation is equal to integral number of switching period.

This phenomenon is shown in Fig. 36.

Lu shows the positive slope of the inductor current and the slope is determined by the input voltage and the primary inductance value of the transformer. -Ld shows the negative slope of the inductor current and the slope is determined by the rate of energy discharge to the secondary side.

Fig. 36 indicates inductor current waveform in the case where T shows the oscillation period and Is shows the control signal of peak inductor current. TON and TOFF are varied even with the same T, Is, Lu and -Ld.

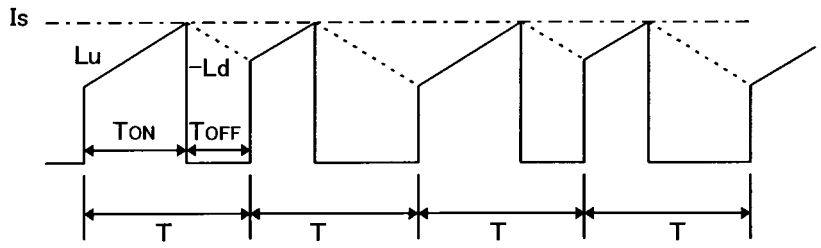


Fig. 36

If it is assumed in Fig. 37 that the inductor current varies Δ iL at t0, the variation Δ iL' of inductor current at t1 is larger than Δ iL at t0. Thereafter, this inductor current variation is gradually increases. As a result , subharmonic oscillation occurs.

Fig. 38 indicates a case when the inductor current variation Δ iL' at t1 is smaller than Δ iL at t0. In this case, this inductor current variation is gradually converged and the inductor current will be stable.

It is necessary to apply slope compensation to control signal in order to prevent from such subharmonic oscillation when the inductor current is continuous and the duty cycle is over 50%.

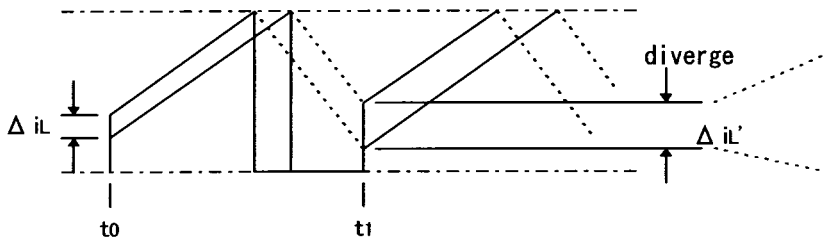


Fig. 37

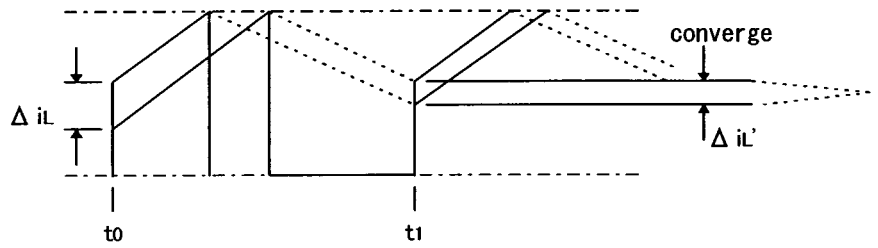


Fig. 38

The waveform of inductor current when slope compensation is applied is shown in Fig. 39 . Slope compensation is adding negative slope of inclination -Kc to the control signal of inductor peak current.

Δ iL ' shows the variation of inductor current at t1 when slope compensation is not applied,

and Δi_L's shows the variation of inductor current at t1 when slope compensation is applied. Thus, Δi_L' can be changed by -Kc, and ΔI_L's becomes smaller when -Kc is large. It is necessary to apply slope compensation so that the equation of $\Delta i_L \geqq \Delta i_L$'s is satisfied to achieve stable operation, that is, the equation of $-Kc \geqq -1/2Ld$ should be satisfied.

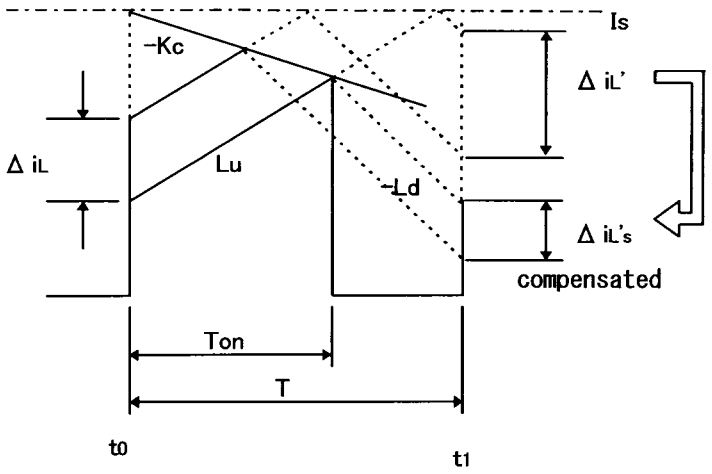


Fig. 39

Typical circuits are shown in Fig. 40 and 41.

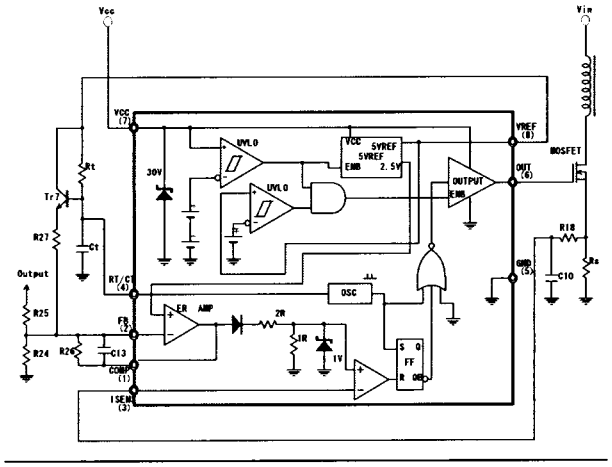


Fig. 40

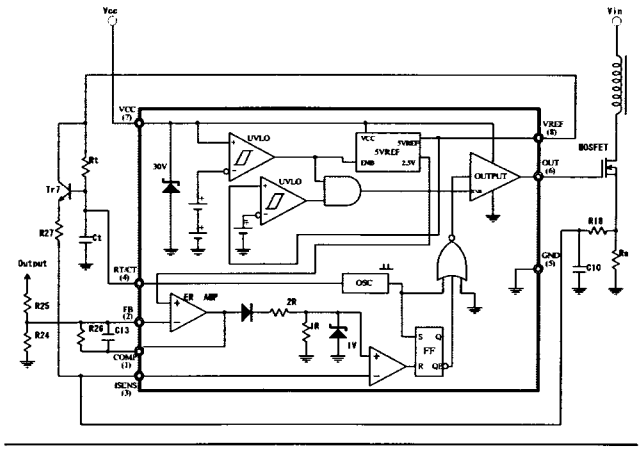
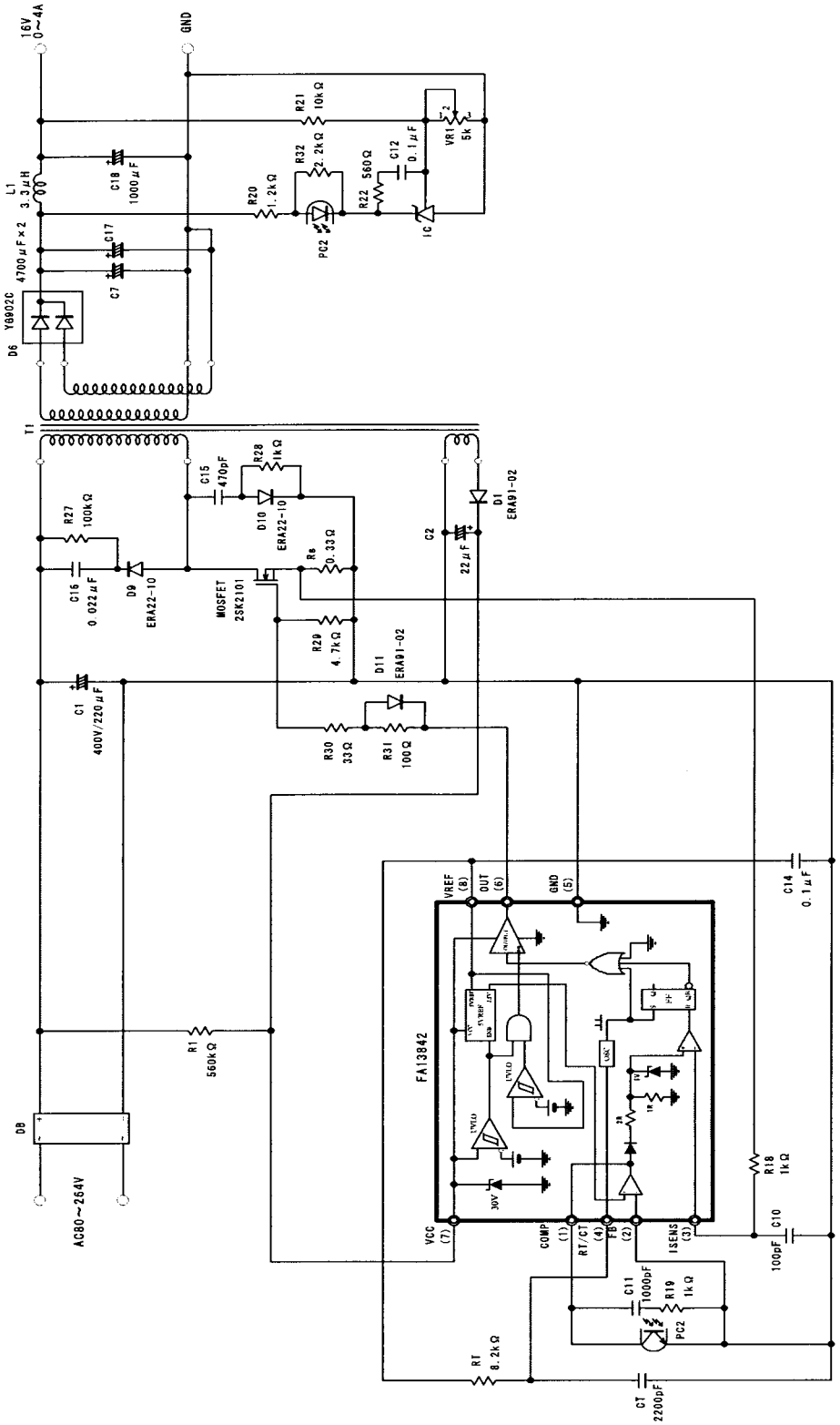


Fig. 41

10. Example of application circuit



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