Fuji Switching Power Supply Control IC

FA5553／54／66／67

Application Note

July '07
Fuji Electric Device Technology Co., Ltd.

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   - Industrial robot etc.

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   - Undersea communication equipment - Medical equipment.

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Contents

Caution)

- The contents of this note subject to change without notice due to improvement.
- The application examples or the parts constants in this note are shown to help your design. Variation of parts and service condition are not fully taken into account. Before use, a design with due consideration for these variations and conditions shall be conducted.

1. Overview

FA5553/54/66/67 is a current mode type switching power supply control IC possible to drive a power MOSFET directly. Despite of a small package with 8 pins, it has a lot of functions and it is best suited for power saving at the light load and decreasing external parts. Moreover it enables to realize a reduced space and a high cost-performance power supply.

2. Features

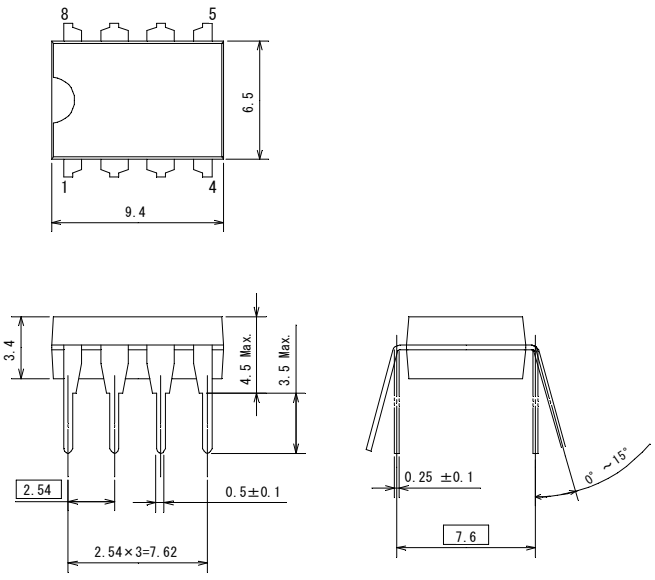
- Possible to improve the efficiency by lowering the oscillation frequency depending on the load at light load.
- Possible to realize low power consumption with a built-in startup circuit.
- Possible to realize the protective operation with little parts due to the built-in overload protection function and built-in over voltage protection function.
- For the overload protection two types are lined up, an auto restart type and a latch shutdown type.
- Possible to adjust both the time up to shutdown of overload protection and the time up to auto restart.
- As the current detection is performed in minus polarity, it is easy to compensate the input voltage at the overload operating point.
- Possible to carry out the protection operation for the application purpose with a built-in latch mode shutdown circuit using an external signal.
  Being shifted to the latch mode by pull-down, it is best suited for the overheat protection using a thermistor.
- Furnishing a built-in drive circuit possible to drive a power MOSFET directly.
  Output current: 1.0 A (sink) / 0.5 A (source)
- Furnishing a built-in low voltage malfunction protection circuit.

Function list

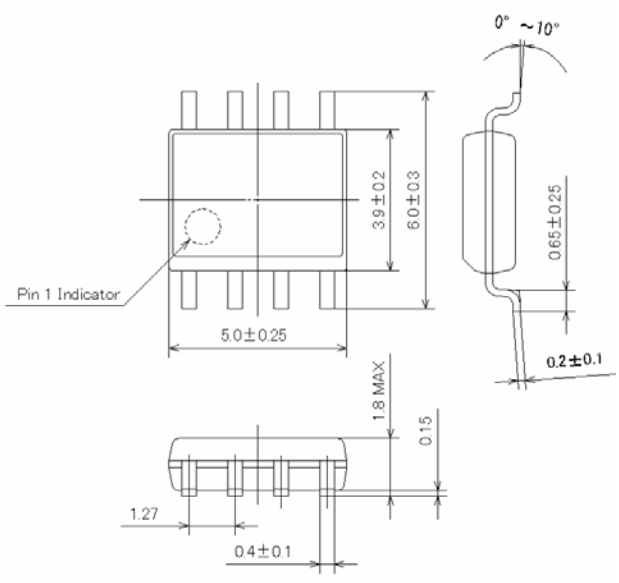
Type	Oscillation frequency	Overload protection
FA5553	60kHz (typ)	Auto restart
FA5554	60kHz (typ)	Timer latch
FA5566	100kHz (typ)	Auto restart
FA5567	100kHz (typ)	Timer latch

3. Outline drawing

DIP-8

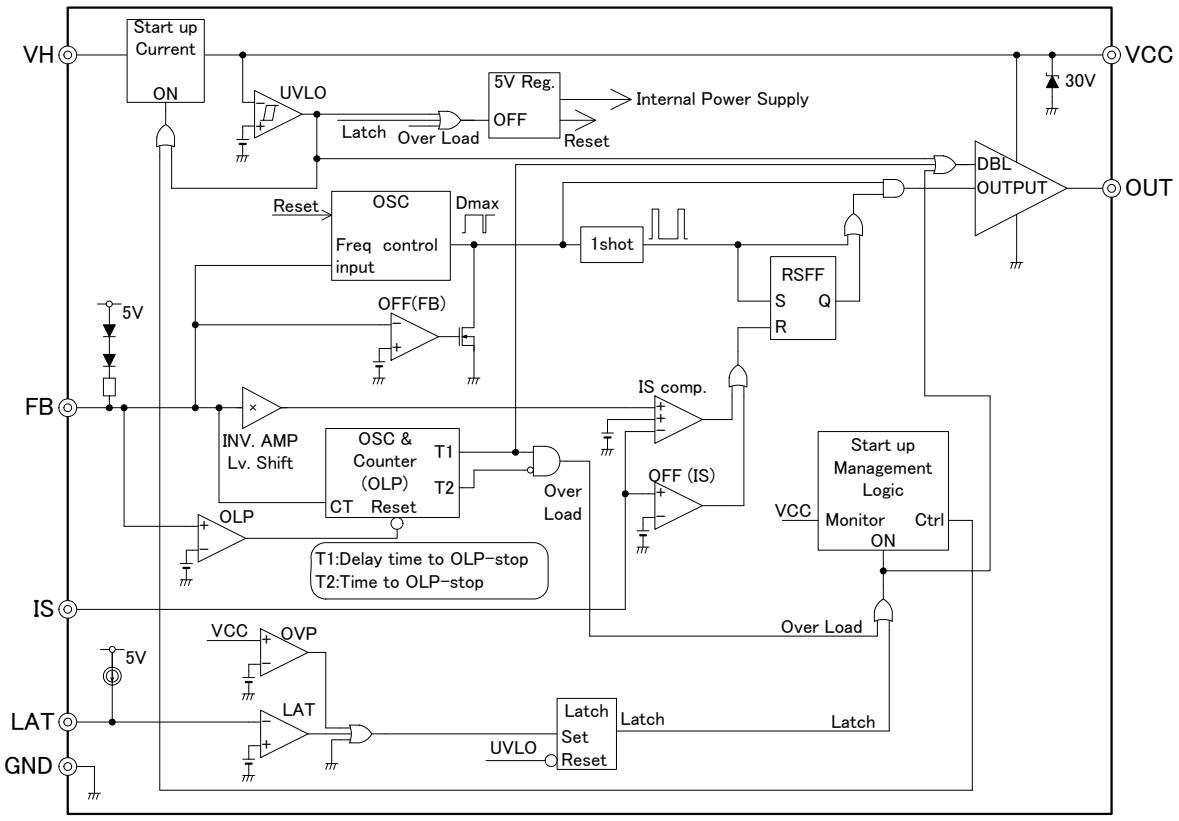


SOP-8

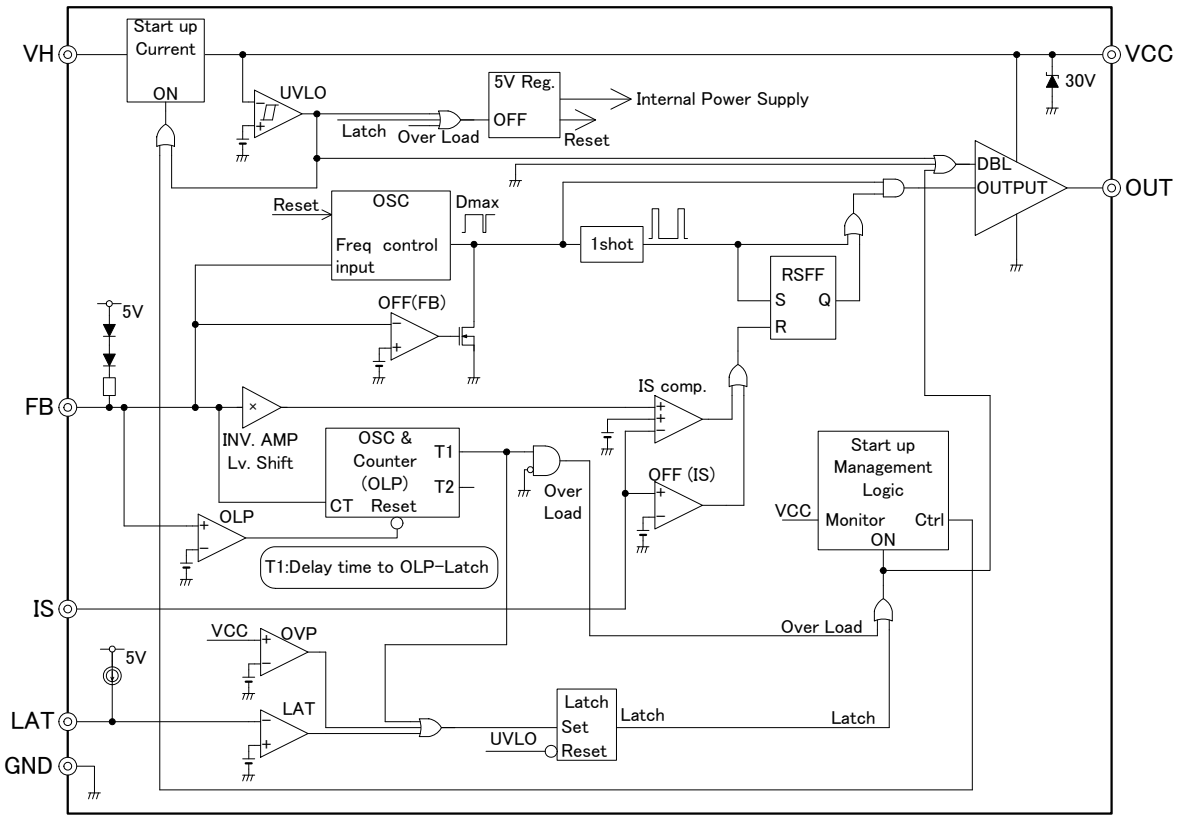


4. Block diagram

FA5553 / FA5566 (Overload protection : Auto restart type)

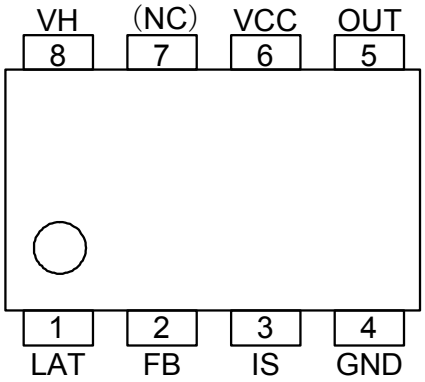


FA5554 / FA5567 (Overload protection : Latch shutdown type)



5. Functional description of pins

Pin No.	Pin Name	Pin function
1	LAT	External latch signal input
2	FB	Feed back input Overload protection timer
3	IS	Current sense
4	GND	Ground
5	OUT	Output
6	VCC	Power supply
7	(NC)	(unused)
8	VH	High voltage input (500Vmax.)



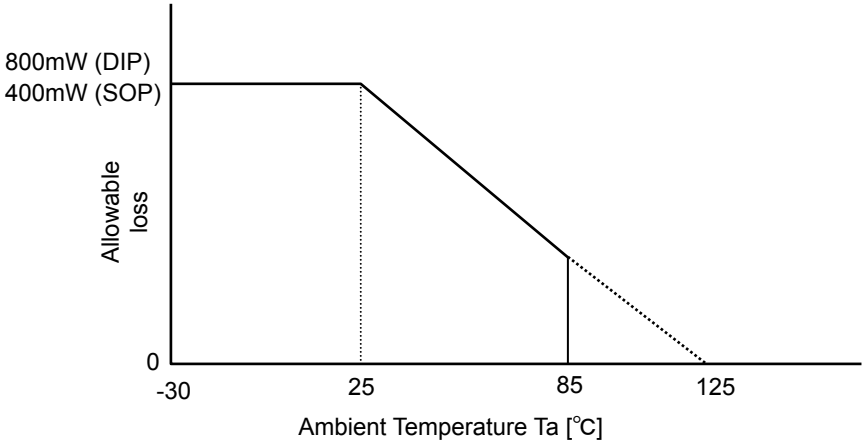
6. Rating & characteristics

* "+" shows sink and "–" shows source in current prescription.

(1) Absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	V_{CC}	28	V
OUT pin output peak current	Ioh	-0.5	A
	Iol	+1.0	A
OUT pin voltage	Vout	-0.3 to Vcc+0.3	V
FB pin voltage	Vfb	-0.3 to 10	V
IS pin voltage	Vis	-5 to 5	V
LAT pin voltage	Vlat	-0.3 to 5	V
VH pin input voltage	Vvh	-0.3 to 500	V
Total loss (Ta = 25℃)	Pd	800 (DIP-8)	mW
		400 (SOP-8)	mW
Junction temperature in operation	Tj	-30 to 125	℃
Storage temperature	Tstg	-40 to 150	℃

○Allowable loss reduction characteristics



(2) Recommended operating condition

Item		Symbol	MIN	TYP	MAX	Unit
VCC Power supply voltage		Vcc	11	18	22	V
High input voltage	Direct current	Vvh(DC)	80		450	V(DC)
	Half-wave rectification	Vvh(AC1)	80		288	V(AC)
	Full-wave rectification	Vvh(AC2)	80		288	V(AC)
LAT pin capacity		Clat	0.22	1.0	2.2	μF
FB pin connection OLP timer capacity		Ctolp	0.01		1	μF
VCC pin capacity		Cvcc	10	33	100	μF
Operating ambient temperature		Ta	-30		85	℃

(3) Electric characteristics (in case nothing specified : Tj=25℃, Vcc=18V)

Oscillator (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Oscillation frequency	Fosc	FA5553/54 : FB=3V	54	60	66	kHz
		FA5566/67 : FB=3V	90	100	110	kHz
Power supply voltage stability	Fdv	Vcc : 11V to 22V	-2	—	+2	%
Temperature stability	Fdt	Tj= -30 to 125℃	-5	—	+5	%
FB voltage at frequency decreasing started	Vfbm		0.75	0.9	1.05	V
Frequency decreasing ratio	kf	FA5553/54 : Δf/ΔVfb	300	375	450	kHz/V
		FA5566/67 : Δf/ΔVfb	410	640	770	kHz/V
Lowest frequency	Fmin		0.22	0.34	0.50	kHz

External latch shutdown signal (LAT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
LAT pin source current	Ilat	DIP:LAT=1.1V	-84	-70	-60	μA
		SOP:LAT=1.1V	-80	-70	-60	μA
External latch shutdown level	VthLAT		1.00	1.05	1.10	V
Latch delay time	TdLAT		55	85	115	μs

Pulse width modulator (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Maximum DUTY cycle	Dmax	FB=3V	75	80	85	%
Minimum DUTY cycle	Dmin	FB=0V	—	—	0	%
Pulse shutdown FB voltage	VthFB0	DUTY=0%	340	400	460	mV
FB pin source current	Ifb0	FB=0V	-300	-250	-200	μA

Overload protection (OLP) circuit part (FB pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Overload detection voltage	VthOLP		2.3	2.5	2.7	V
Overload delay circuit charging current	Ichg2	FB=7V	-80	-55	-40	μA
Overload delay circuit discharging current	Idchg2	FB=6V	16	27	38	μA
Overload delay circuit Threshold level	Vhosc2	OLP mode	7	8	9	V
	Vlosc2	OLP mode	3.8	4.7	5.6	V
Overload timer counted number	NCNT1	Number counted till OLP (latch) shutdown * common to 4 types	—	5	—	counted number
	NCNT2	Number counted till VH pin current shutdown *FA5553/66 only	—	33	—	counted number

Current sense (IS pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Voltage gain	AvIS	ΔVFB/ΔVIS	-1.8	-1.5	-1.2	V/V
Maximum input threshold voltage	VthIS1	FB=3V	-1.05	-0.95	-0.85	V
Input bias current	IIS	IS=0V	-26	-20	-14	μA
Minimum ON width	Tmin	FA5553/54	570	720	870	ns
		FA5566/67	400	520	640	ns
Output delay time	TpdIS		100	200	300	ns

VCC circuit (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
ON threshold voltage	VCCon		16	18	20	V
OFF threshold voltage	VCCoff		8.8	9.8	10.8	V
Hysteresis width	Vhys		6.8	8.2	9.6	V
Over voltage protection threshold voltage	Vthovp		22.5	24	25.5	V

Output (OUT pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
L output voltage	VOL	IOL=100mA, VCC=18V	0.4	0.8	1.6	V
H output voltage	VOH	IOH= -100mA,VCC=18V	14.5	16.5	17.5	V
Rise time	tr	CL=1nF	20	40	100	ns
Fall time	tf	CL=1nF	15	30	70	ns

High voltage input (VH pin, VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
VH pin input current	IHrun	VH=450V VCC pin > VCCon	10	35	60	μA
	IHstb	VH pin=100V、 VCC pin=0V	4.0	6.7	9.6	mA
Latch VCC voltage	VCCLH	VH pin=100V upper level	12	13.4	15	V
	VCCLL	VH pin=100V lower level	11	12.2	14	V
VCC pin charging current	Ipre1	VCC pin=16V、 VH pin=100V	-8.9	-5.8	-3.1	mA
	Ipre2	VCC pin=11V、 VH pin=100V (at Latching)	-9.0	-6.2	-3.7	mA

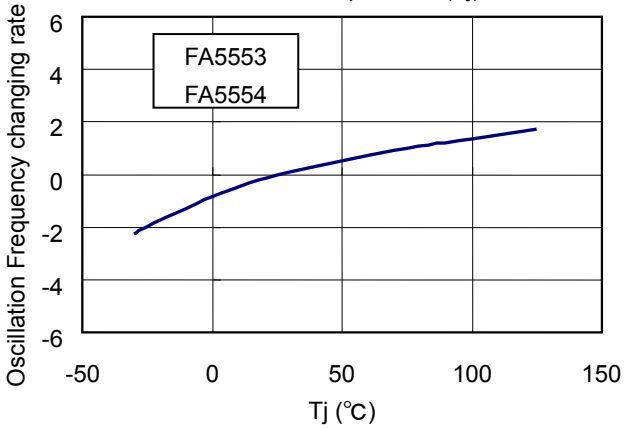
Power supply current (VCC pin)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Operational power supply current	ICCop1	Duty cycle=Dmax FB=2V、OUT=No Load		1.35		mA
	ICCop2	Duty cycle=0% FB=0V		1.33		mA
Latch power supply current	ICClat	FB=open		0.46		mA
Power supply Zener voltage	VCCzd	Iz=2mA * built in Zener		30		V

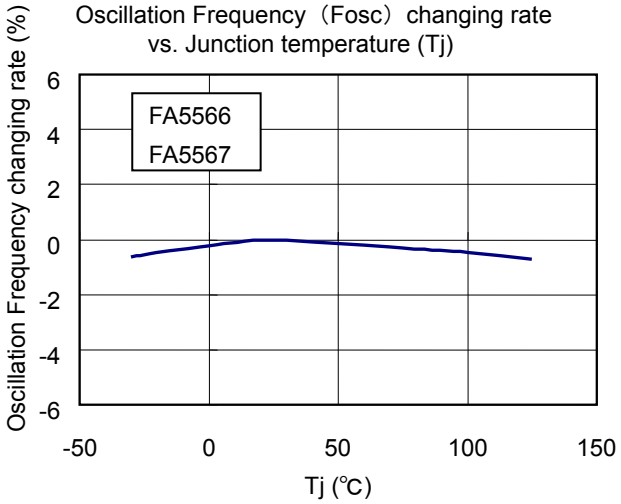
7. Characteristics curve

- In case nothing is specified otherwise: Ta=25℃, VCC＝18V
- "+" shows sink and "–" shows source in current prescription.
- Data written here show the typical characteristics of the IC and do not guarantee the characteristics.

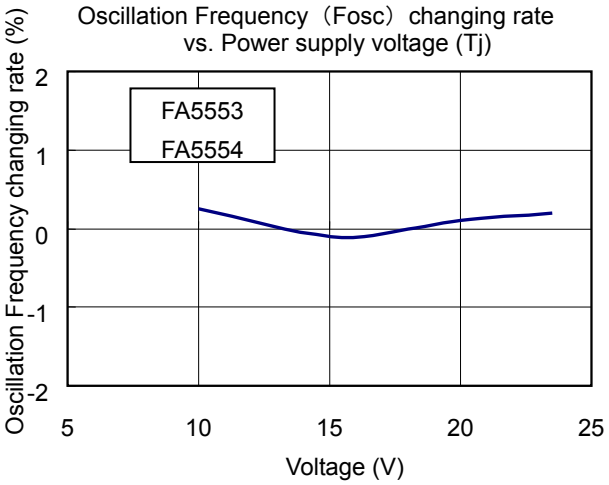
Oscillation Frequency（Fosc）changing rate vs. Junction temperature (Tj)



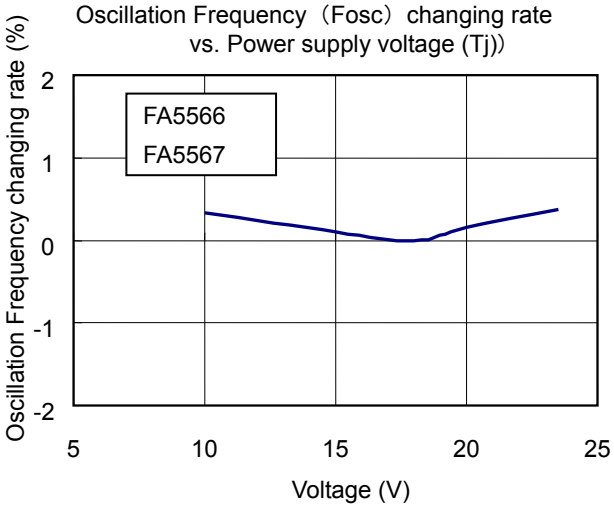
Oscillation Frequency（Fosc）changing rate vs. Junction temperature (Tj)



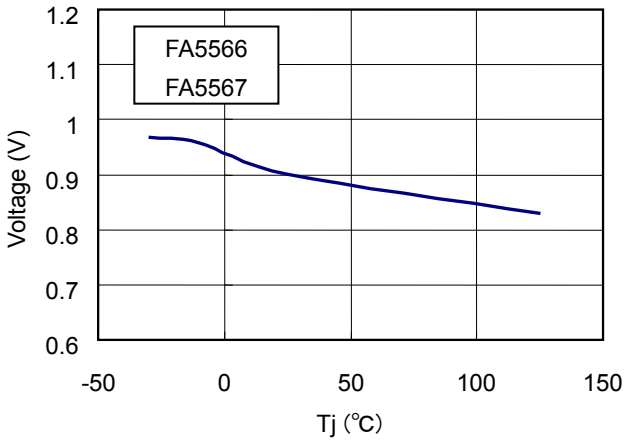
Oscillation Frequency（Fosc）changing rate vs. Power supply voltage (Tj)



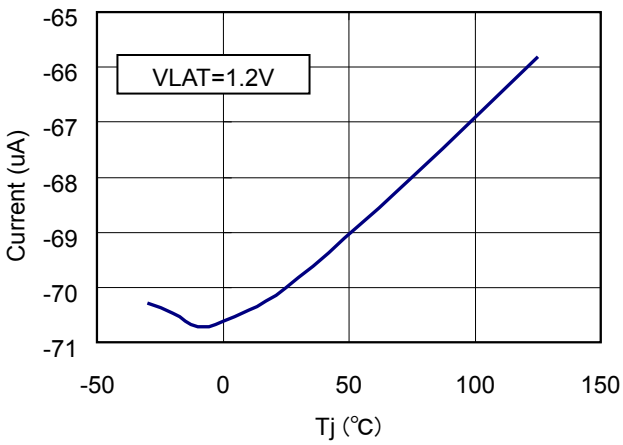
Oscillation Frequency（Fosc）changing rate vs. Power supply voltage (Tj))



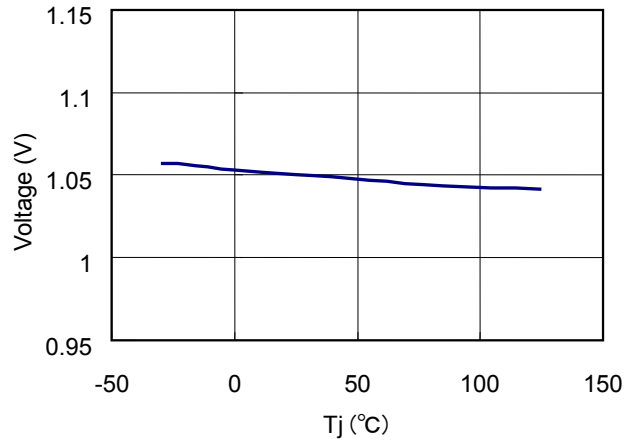
FB pin voltage（Vfbm）at frequency drop started vs. Junction temperature (Tj)



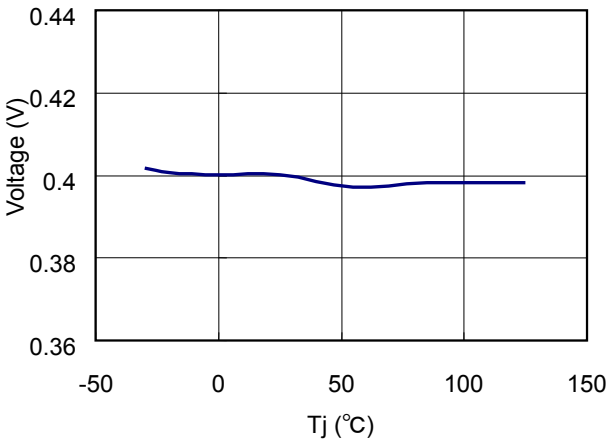
LAT pin source voltage（Ilat） vs. Junction temperature (Tj)



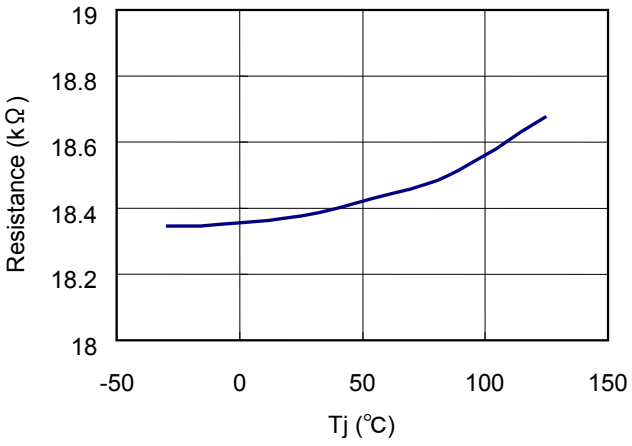
Latch cutoff threshold Voltage (VthLAT)
vs. Junction temperature (Tj)



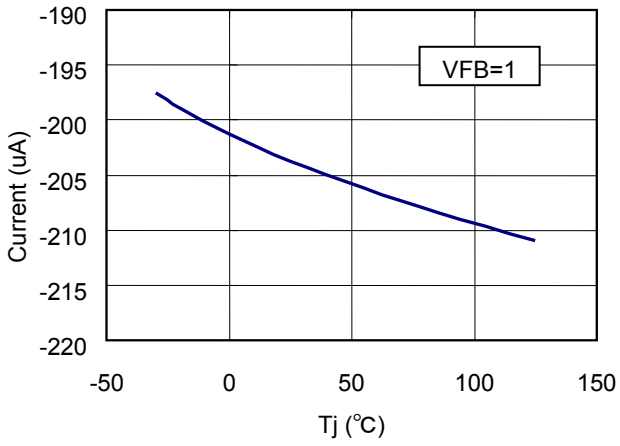
Output shutdown threshold voltage (VthFB0)
vs. Junction temperature (Tj)



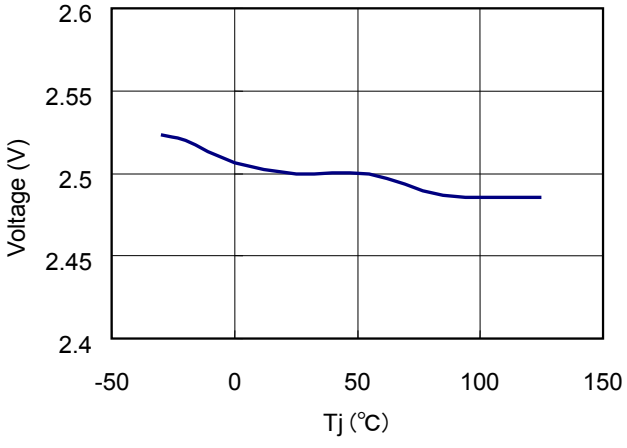
FB pin input resistance (Rfb)
vs. Junction temperature (Tj)



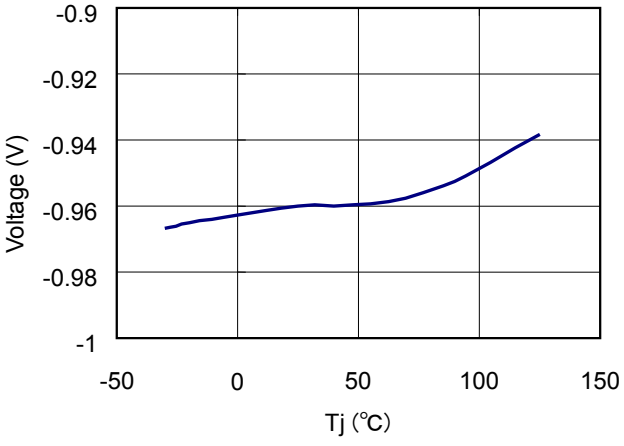
FB pin source current（IFB）
vs. Junction temperature (Tj)



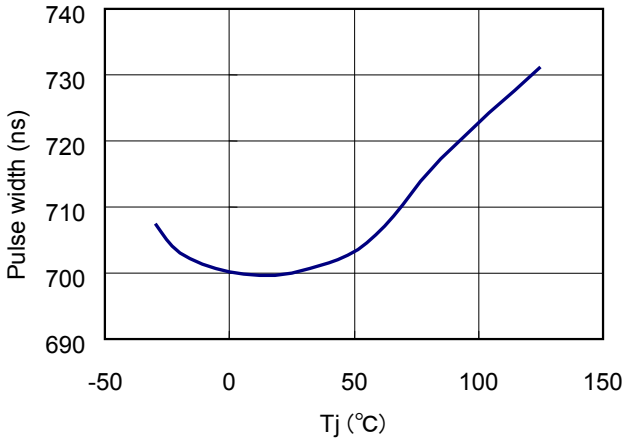
OLP detection voltage (VthOLP)
vs. Junction temperature (Tj)



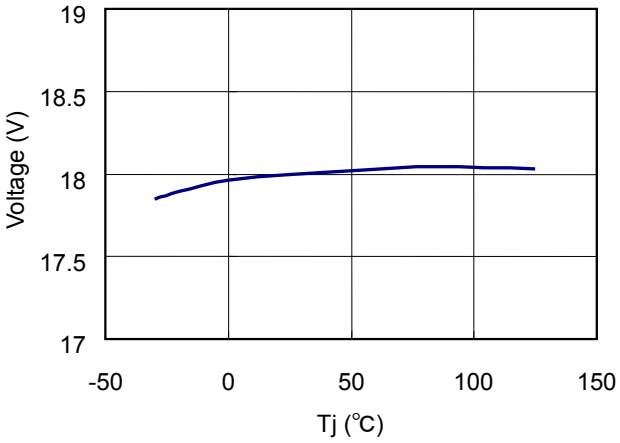
Current sense maximum input threshold voltage (VthIS)
vs. Junction temperature (Tj)



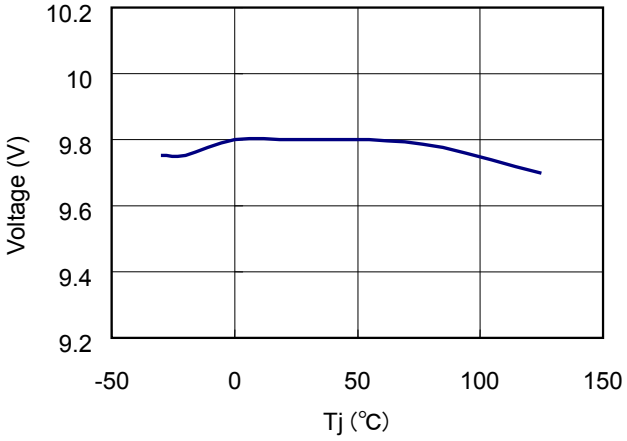
Minimum ON width (Tmin)
vs. Junction temperature (Tj)



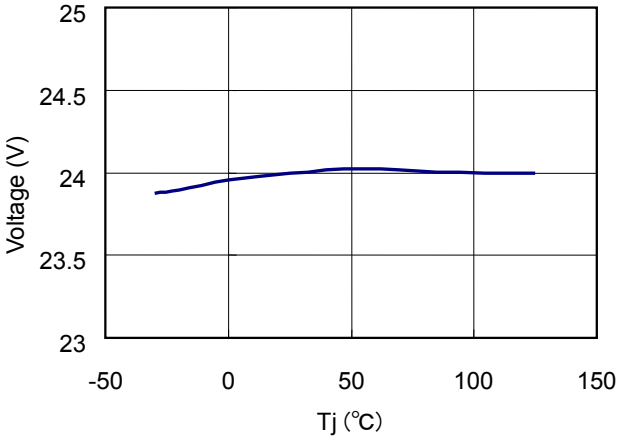
UVLO release threshold voltage (VCCon)
vs. Junction temperature (Tj)



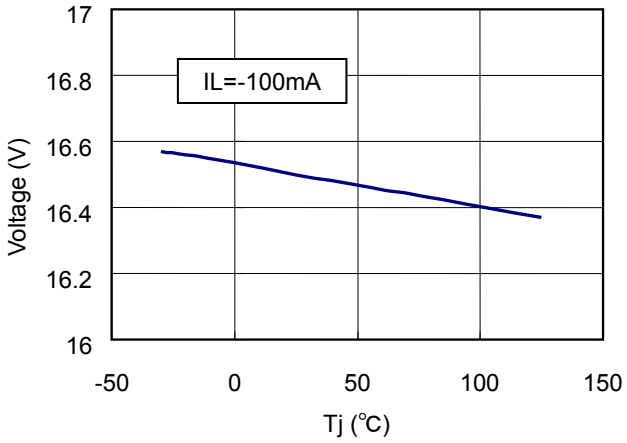
UVLO activate threshold voltage (VCCoff)
vs. Junction temperature (Tj)



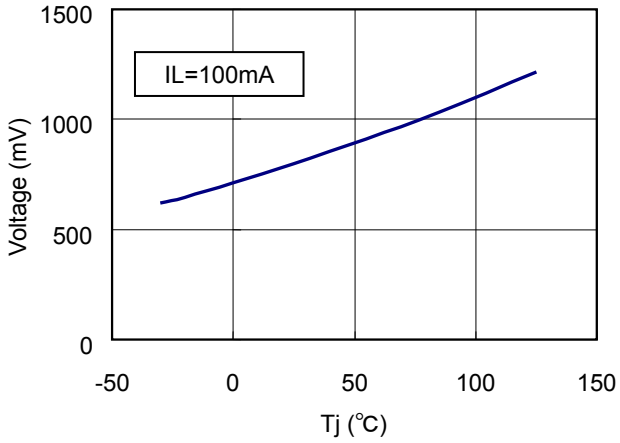
Overvoltage threshold voltage (VthOVP)
vs. Junction temperature (Tj)



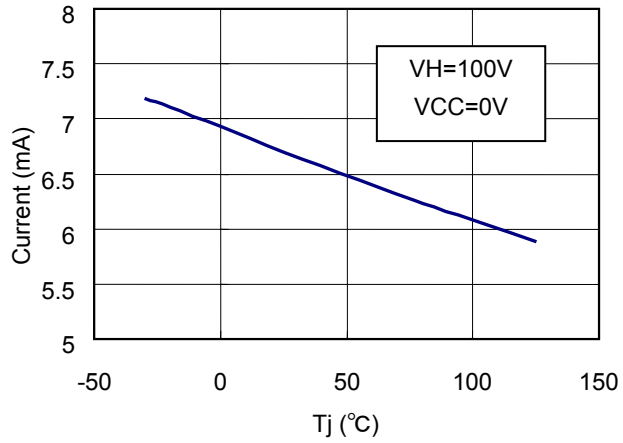
Output voltage high level (VOH)
vs. Junction temperature (Tj)



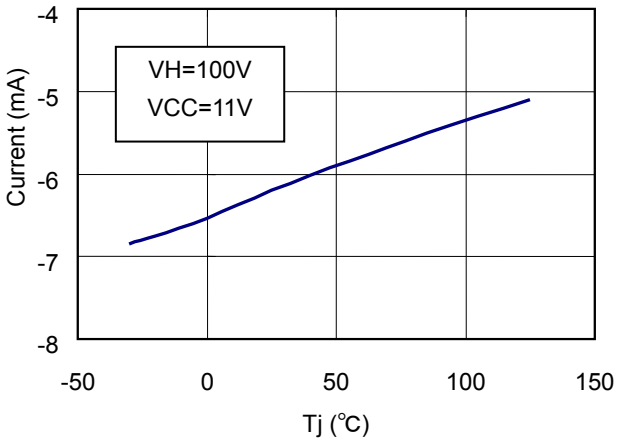
Output voltage low level (VOL)
vs. Junction temperature (Tj)



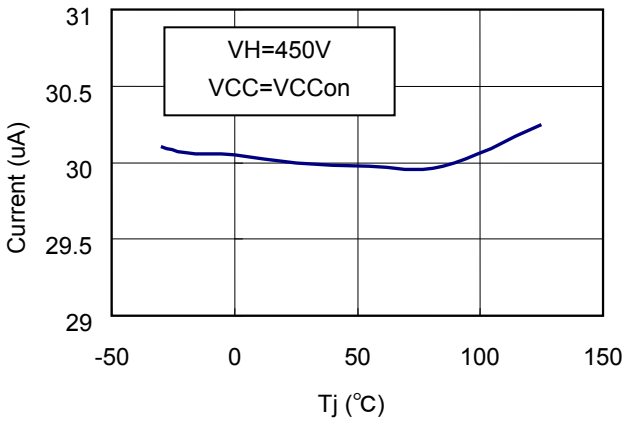
VH pin Input current (IHstb)
vs. Junction temperature (Tj)



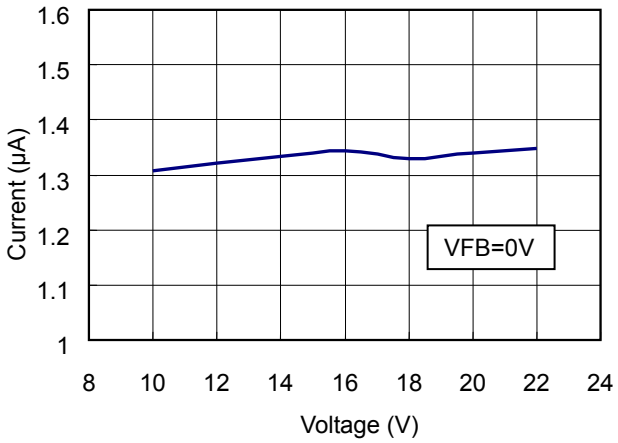
VCC pin capacity charge current (Ipre2)
vs. Junction temperature (Tj)



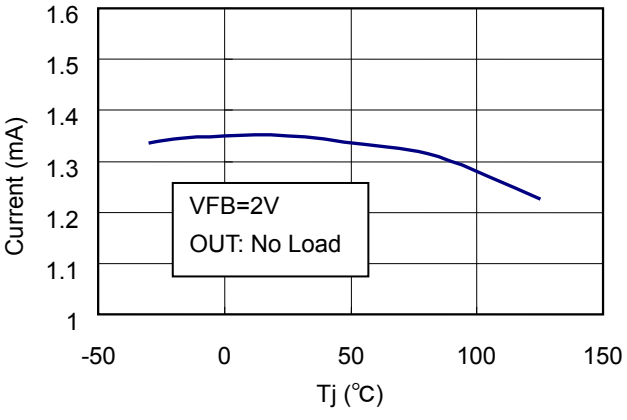
VH pin Input current (IHrun)
vs. Junction temperature (Tj)



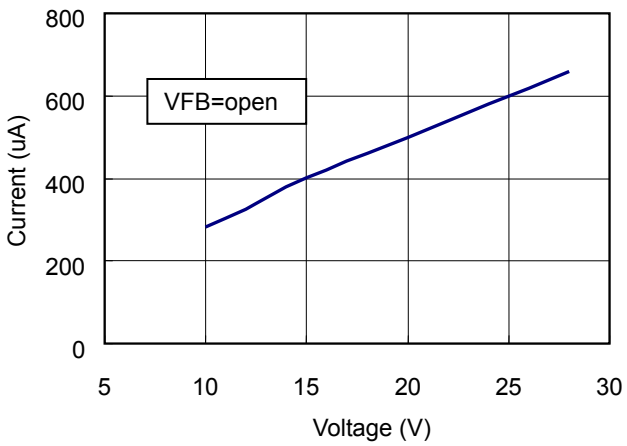
Operational power supply current (ICCop2)
vs. VCC pin voltage (VCC)



Operational power supply current (ICCop1)
vs. Junction temperature (Tj)



Latch power supply current (ICClat)
vs. VCC pin voltage (VCC)



8. Operation of each block

(1) Startup circuit

FA5553/54/66/67 has a startup circuit in it. Its absolute maximum rating is 500V.

Fig.1 to Fig.3 shows the connection.

Turning on the power, capacitor C2 connected to VCC pin is charged and its voltage rises due to the current provided from the startup circuit to VCC pin. And the IC starts up and the power supply begins to operate.

The current provided from VH pin to VCC pin is about 7 mA when Vcc is 0V. As Vcc rises, the provided current decreases and gets to about 5.8 mA at the startup voltage.

A resistor should be connected in series to VH pin to prevent the damage of the IC by surge voltage on AC line.

Fig.1 shows the most popular connection where VH pin is connected to the half-wave rectification circuit of AC input voltage.

Therefore the startup time of this connection is the longest in 3 types of connection. However, if AC input voltage is shutdown after the IC goes into latch mode, the current provided from VH pin runs out by overload protection or over voltage protection and latch mode can be reset in a short time like several seconds.

Fig.2 shows the connection where VH pin is connected to the full-wave rectification circuit of AC input voltage. This connection makes the startup time short about half comparing with that of half-wave rectification in Fig.1 and also the reset of the latch mode can be done in a short time as Fig.1

Fig.3 shows the connection where VH pin is connected to the back of rectification and smoothing of AC input voltage. The startup time of this connection is the shortest in 3 types. But in this connection, even if AC input voltage is shutdown after the IC goes into latch mode, it takes much time to reset the latch mode because the voltage charged in C1 is impressed to VH pin. Note that depending on the service condition, it takes generally several minutes after AC input is shutdown.

If VCC pin voltage exceeds ON threshold voltage of a low voltage malfunction protection circuit and the IC begins to operate, the startup circuit becomes to shutdown state and the current to VH pin gets to 35μA (typ.).

If the overload protection or the over voltage protection operates and the IC goes into latch mode, the startup circuit is ON/OFF controlled to maintain the latch state and VCC voltage is kept between 13.4V (typ.) and 12.2V (typ.).

(See page 17, 18 "8-(5) & (6) Overload protection", and page 19 "8-(7) Overvoltage protection").

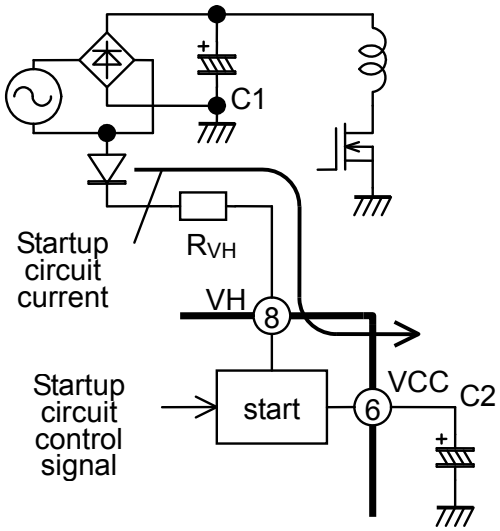


Fig.1 Startup circuit 1 (Half-wave)

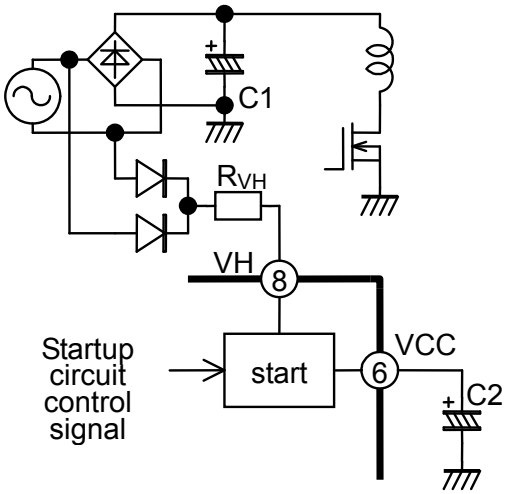
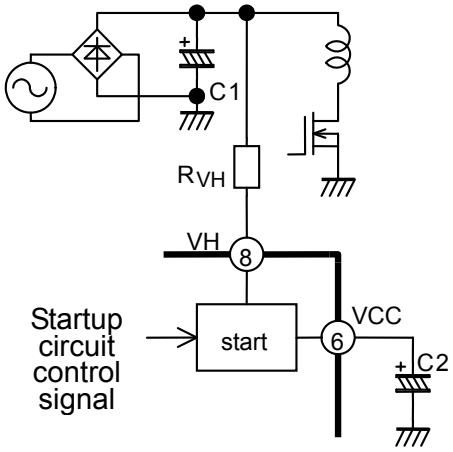


Fig.2 Startup circuit 2 (Full-wave)



※Caution: Connection in Fig.3 requires a few minutes for resetting Latch mode.

Fig.3 Startup circuit 3 (Rectification)

(2) Oscillator

This oscillator fixes switching frequency.
Switching frequency is set in the IC as below in the normal operation mode.
FA5553/54 : 60kHz,　　FA5566/67 : 100kHz

Moreover this IC has the function to lower switching frequency automatically at light load in order to reduce the power supply loss at the standby state. Frequency reduction at light load is in proportion to FB pin voltage and decreases almost linearly to the minimum frequency (Fig.4). The minimum frequency Fmin is set to 0.35kHz (typ.).

In addition, this oscillator generates a pulse signal that fixes the maximum duty cycle and a ramp signal that compensates slope as well as a trigger signal that fixes switching frequency.

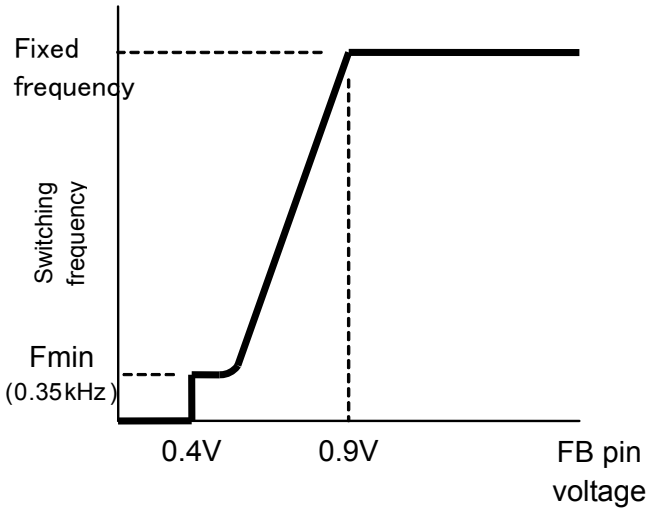


Fig.4 Oscillation frequency

(3) Current comparator & PWM latch circuit

FA5553/54/66/67 performs current mode control.
A circuit block of its basic operation is shown in Fig.5 and a timing chart in Fig.6.

A trigger signal for switching frequency that is output from an oscillator is input into PMW latch (F.F.) through 1 shot circuit as a setting signal. Then the output of PMW latch gets to High state and also OUT pin voltage gets to High state.
On the other hand, a current comparator (IS comp) monitors the current of MOSFET and if the current gets to the threshold voltage, a reset signal is output. The output of PWM latch (F.F.) gets to Low state with the input of a reset signal and OUT pin voltage also gets to Low state.

The output is controlled by changing the threshold voltage of this IS comp with a feedback signal.

FB pin voltage is level-shifted by a reverse amplifier and is input into a current comparator (IS comp.) as the threshold voltage as shown in Fig.7. In addition, the standard voltage of –0.95V is input inside of the IC to regulate the maximum input threshold voltage of IS pin.
Higher voltage out of these two inputs has priority as the threshold voltage.
(Ex. When the output of a reverse amplifier is –0.5V, if IS pin voltage gets to –0.5V, the current comparator is reversed.)

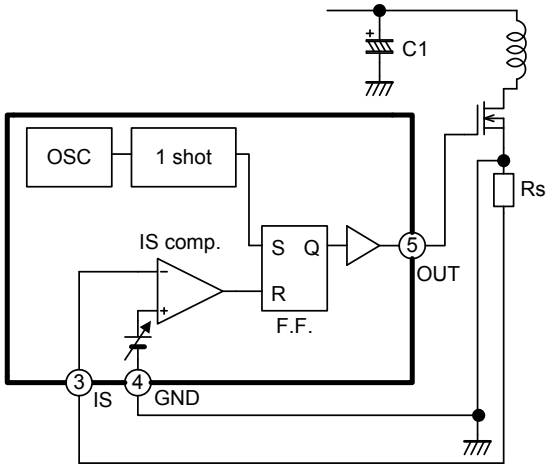


Fig.5 Current mode basic operation circuit block

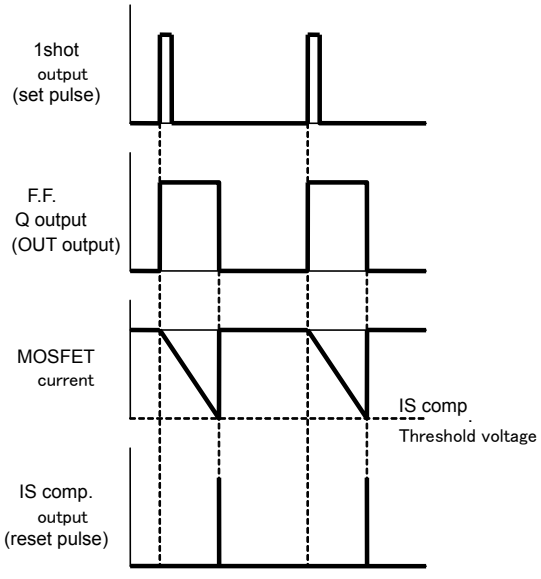


Fig.6 Current mode basic operation timing chart

In normal operation, the output voltage of a power supply is kept constant by changing the threshold voltage of the current comparator via FB pin voltage.
The maximum value is set for the threshold voltage of IS pin and that enables to control over-current of MOSFET. When FB pin voltage rises due to overload etc., the output of reverse amplifier will scale out to Low and gets lower than '–0.95V'. Consequently the maximum threshold voltage of IS pin gets to '–0.95V (typ.)'.

An oscillator outputs pulses that define the maximum duty cycle of OUT pulse. Using this pulse, the maximum duty cycle is set 80% (typ.).

(4) One shot circuit (minimum ON width)

When the MOSFET turns on, a surge current occurs due to the discharge corresponding to the capacitance of a main circuit and gate drive current. If this surge current gets to IS pin threshold voltage, the current comparator output is reversed and normal pulses may not be generated from OUT pin.
To avoid this, a minimum ON width of OUT pin output is set in the one shot circuit block of the IC.
If a trigger signal of switching frequency is input from an oscillator, a pulse with definite width is output as a set signal for PWM latch (F.F.).
The set signal has priority over an input signal of PWM latch. Therefore while a set signal is being input from a blanking circuit, the output of PWM latch (F.F.) is not reversed even if s reset signal is input from the current comparator (IS comp.).
Consequently input for IS pin becomes invalid and does not respond to the surge current at turn-on for a period soon after output pulses are output from OUT pin. (minimum ON width, FA5553/54 : 720ns, FA5566/67 : 520ns) (See Fig.8).

Generally a noise filter of IS pin is unnecessary because of this minimum ON width function.

In addition, an exclusive comparator is built-in to make output pulse zero at no load.
This comparator reverses its output when FB pin voltage gets to 400mV (typ.) or less. After that a set pulse is not output from one shot circuit. Consequently the set signal is not input into PWM latch (F.F.) and the output is kept at Low state. (See Fig.9)

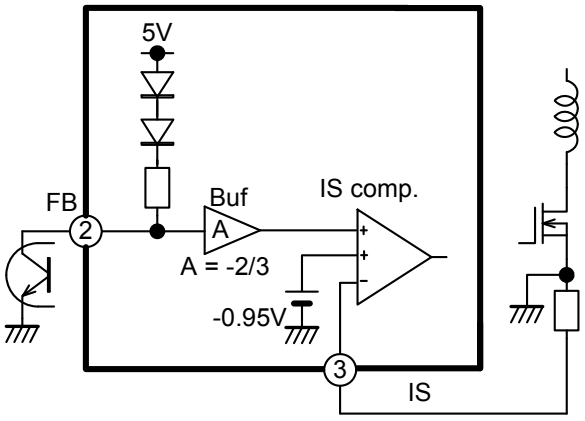


Fig.7 Current comparator

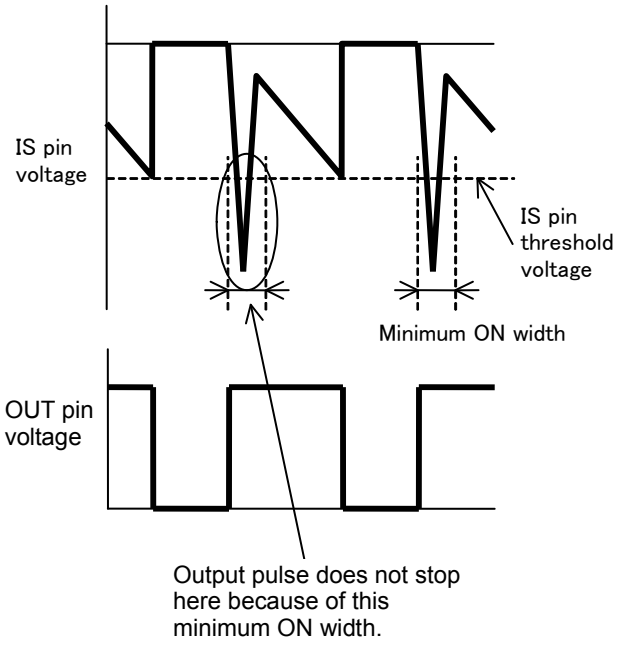


Fig.8 Minimum ON width

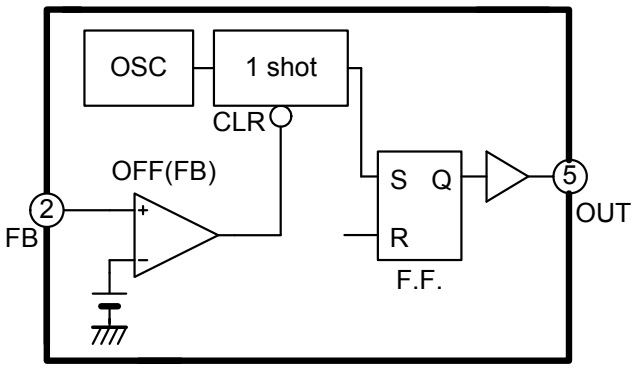


Fig.9 Output shutdown function of FB pin

(5) Overload protection circuit (FA5553 / FA5566)

FA5553/FA5566 has auto restart type overload protection in it. Its circuit block is shown in Fig.10 and the timing chart of protection operation in Fig.11.

If overload is detected by monitoring FB pin voltage, a built-in oscillator for OLP and a counter are activated.
This counter uses a time constant as a clock, and the time constant is get from the oscillator for OLP when it charges and discharges the capacitor connected to FB pin with constant current.
The delay time up to switching pulse shutdown after detecting overload and the stop time from switching shutdown to restarting of auto restart operation are adjustable with connection capacity of FB pin.
However time ratio between the delay time and the time up to restarting is fixed in the IC.

The flow of the auto restart operation is explained below.

- The load current increases and FB pin voltage rises.
- If FB pin voltage rises more than 2.5V (typ.), the oscillator for OLP begins to operate, and reset of a counter is canceled together. At this time, both output T1 and T2 keep Low level. And OUT pin still outputs pulses and continues PWM control (Fig.11 period 0-1).
- Since the oscillator for OLP charges and discharges with different constant current between 4.7V (typ.) and 8V (typ.), FB pin voltage changes like a saw-tooth.
- After FB pin begins to oscillate, when the top of 5th saw tooth is counted, output T1 outputs High level (period 1).
- Once T1 outputs High level, OLP switching is stopped. At the same time, a startup current control circuit begins to operate and controls to keep VCC pin voltage between 12.2V (typ.) and 13.4V (typ.) with ON/OFF control of startup current (period 2).
- After T1 outputs High level, OLP counter still continues to count. When detecting the top of 33rd saw tooth (totally 38th saw tooth after FB exceeds 2.5V), T2 outputs High level. At that time, output T1 is still kept at High level.
- If both T1 and T2 output High level, the startup current control circuit stops its operation. Then current supply from VH pin to VCC pin is stopped. Consequently VCC pin voltage begins to decrease in proportion to the consumption current of the IC (period 3).
- As a result the IC stops because of UVLO.
- When UVLO becomes effective, a startup current control circuit begins to operate again and the IC starts its operation in the same sequence as the startup sequence.
- Until the load current decreases and the overload state is resolved, the operation mentioned above is repeated. Repetition will finish if FB pin voltage falls lower than 2.5V.

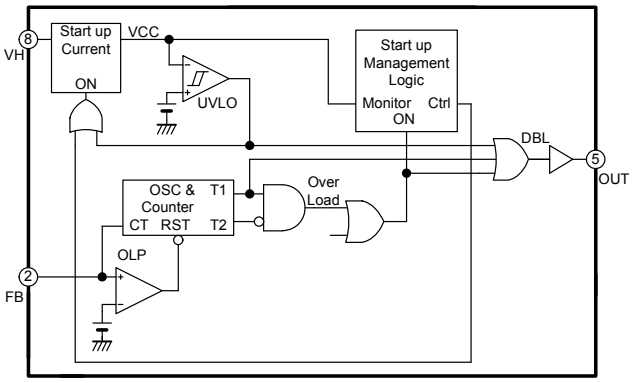


Fig.10 Overload protection circuit (auto restart type : FA5553/FA5566)

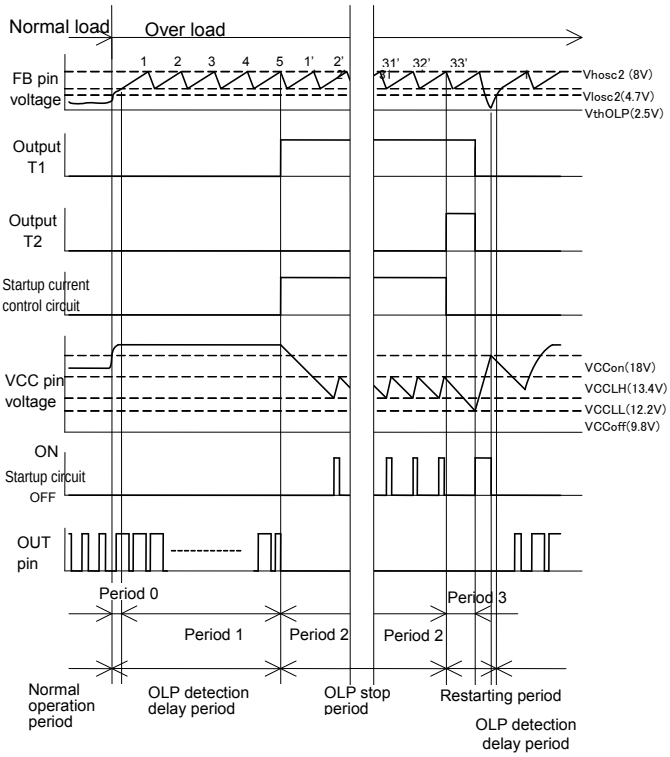


Fig.11 Overload protection timing chart (auto restart type)

(6) Overload protection circuit (FA5554/67)

FA5554/FA5567 has latch shutdown type overload protection in it. Its circuit block is shown in Fig.12 and a timing chart of the protection operation in Fig.13.

If overload is detected by monitoring FB pin voltage, a built-in oscillator for OLP and a counter are activated.
This counter uses a time constant as a clock, and the time constant is get from the oscillator for OLP when it charges and discharges the capacitor connected to FB pin with other different constant current.
The delay time up to switching pulse shutdown after detecting overload is adjustable by connection capacity of FB pin.

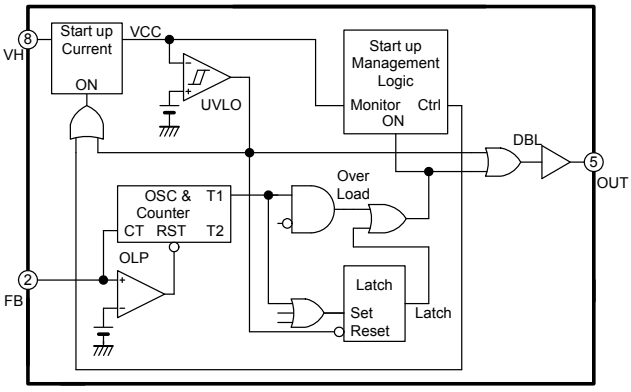


Fig.12 Overload protection circuit (timer latch type : FA5554/67)

The flow for latch mode transition is explained below.

- The load current increases and FB pin voltage rises.
- If FB pin voltage rises more than 2.5V (typ.), the oscillator for OLP begins to operate, and reset of a counter is canceled together. At this time, output T1 keeps Low level. And OUT pin still outputs pulses and continues PWM control (Fig.13 period 0-1).
- Since the oscillator for OLP charges and discharges with different constant current between 4.7V (typ.) and 8V (typ.), FB pin voltage changes like a saw-tooth.
- After FB pin begins to oscillate, when the top of 5th saw tooth is counted, output T1 outputs High level (period 1).
- T1 is input as a set signal for the latch circuit, and the IC transfers into the latch mode at this timing.
- Transferring into the latch mode, the startup current control circuit begins to operate and controls to keep VCC pin voltage between 12.2V (typ.) and 13.4V (typ.) with ON/OFF control of the startup current (period 2).
- This is the operation for maintaining the latch mode and prevents VCC voltage from falling into UVLO.

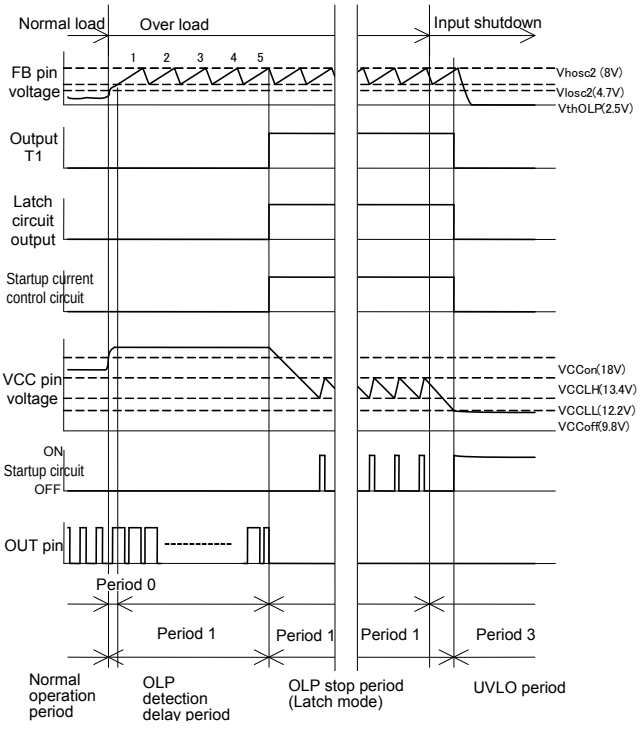


Fig.13 Overload protection timing chart (timer latch type)

It is possible to release the latch mode by shutting down the input voltage because the latch mode is released by UVLO. However, be careful if VH pin is connected after rectification, it takes generally long time such as several minutes to reset the latch mode even after the input voltage is shutdown (See 8-(1) Startup circuit).

(7) Over voltage protection circuit

FA5553/54/66/67 has an over voltage protection circuit that monitors Vcc voltage (See Fig.14).

If Vcc voltage rises and exceeds the standard voltage 24V of a comparator (OVP), the output of the comparator reverses to High level and sets up a latch circuit.
At this time, the startup current control circuit begins to operate and controls to keep VCC pin voltage between 12.2V (typ.) and 13.4V (typ.) with ON/OFF control of the startup current (period 2).
This operation prevents latch from being released due to the drop of Vcc voltage and the transition to UVLO mode.
It is also possible to release the latch mode by shutting down the input voltage and lowering Vcc voltage just like the case of overload protection (latch shutdown type).
However, be careful about the relation between the connection of VH pin and the reset time of the latch mode (See 8-(1) startup circuit).
In addition, 85μs (typ.) delay time is set for the setting input of a latch circuit. Therefore the transition to the latch mode is not possible even if Vcc pin voltage exceeds the detection voltage transitionally.

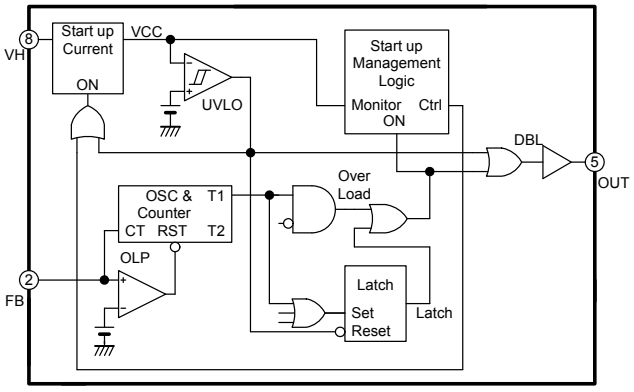


Fig.14 Over voltage protection circuit

(8) Latch shutdown circuit by an external signal

LAT pin of FA5553/54/66/67 has latch shutdown function (See fig.14).
If LAT pin voltage is lowered to 1.05V (typ.) or less, the IC is transferred into the latch mode.
It is possible to release the latch mode by lowering VCC pin voltage and transferring into UVLO mode just like in OVP latch.
However, be careful about the relation between the connection of VH pin and the reset time of the latch mode (See 9-(1) startup circuit).
Latch function of LAT pin becomes effective only after the IC is activated and LAT pin voltage exceeds 1.25V once.
Therefore, if LAT pin voltage is fixed such as pull-down to GND, latch shutdown function is not available.
(* OVP latch function is available.)

-Overheat protection function-

Overheat protection function can be realized by connecting a thermistor to LAT pin for FA5553/54/66/67 (See fig.15).
For farther explanation of this function, refer "9-(8) Latch shutdown function by an external signal")

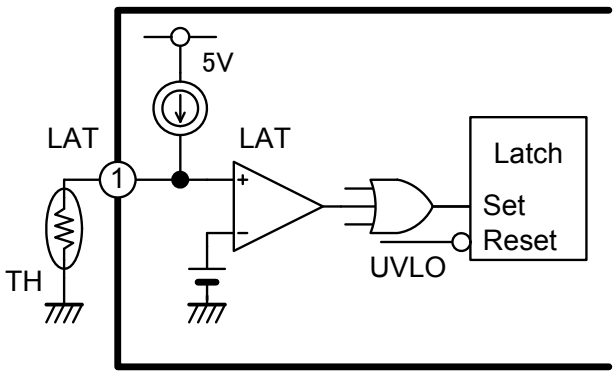


Fig.15 Over temperature protection function using a thermistor

(9) Low voltage malfunction protection circuit

A low voltage malfunction protection circuit is built-in to protect circuit malfunction at the drop of power supply voltage. When Vcc voltage rises from 0V and gets to 18V(typ.), the IC begins its operation. And when Vcc falls and gets to 9.8V(typ.), the IC stops its operation.

When a low voltage malfunction protection circuit works and the IC is stopped its operation, OUT pin is forced to transfer to Low state.

(10) Output circuit

This is push-pull structured output circuit and enables to drive MOSFET directly. As for the output peak current of OUT pin, the absolute maximum rating is specified as 0.5A for source and 1.0A for sink.
In the state when the IC is stopped by the low voltage malfunction protection circuit or it is stopped by the latch protection function or it is waiting for auto restart by overload mode (FA5553/66), OUT pin transfers to Low level and a MOSFET is led to shutdown.

9. Advice for designing

(1) Startup

The capacitance of a capacitor connected to VCC pin must be rightly selected to start and stop a power supply adequately.
VCC voltage at startup is shown in Fig.16 when a right capacitor connected.
If power supply is turned on, the capacitor of VCC is charged by the current provided from the startup circuit and its voltage rises.
When VCC gets to ON threshold voltage, the IC begins to operate. The IC operates with the voltage provided from an auxiliary coil at the steady state. However, immediate after the startup of the IC, VCC decreases until the voltage of an auxiliary coil starts up.
Select VCC capacitor in order that VCC does not fall to OFF threshold voltage in this period.
Practically, VCC pin capacitor that keeps lower limit of VCC higher than 11V is recommendable.

If the capacitance of VCC capacitor is too small, VCC falls to OFF threshold voltage before the auxiliary coil voltage starts up as shown in Fig.17. In this case, VCC repeats up and down between ON threshold voltage and OFF threshold voltage, and a power supply can't be started up.

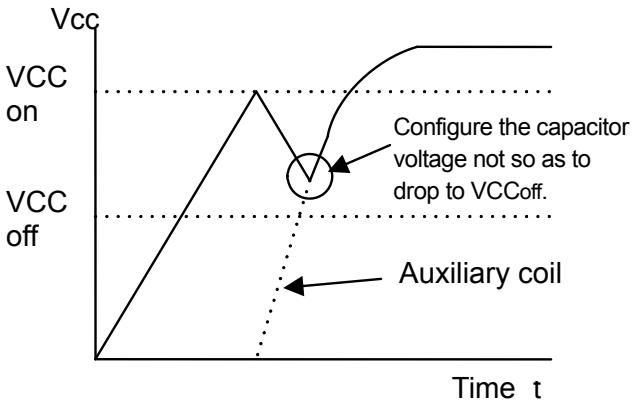


Fig.16 VCC pin voltage at startup

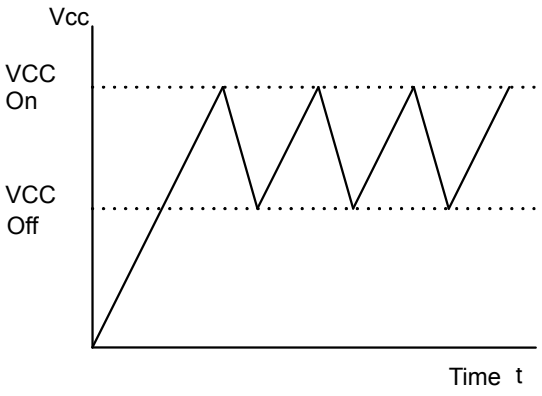


Fig.17 VCC pin voltage at startup (too small capacitance)

(2) VCC hold time

In some cases, big capacitance for VCC pin capacitor is required in order that after a power supply starts up, VCC pin voltage doesn't fall lower than UVLO threshold voltage due to sudden change of the load.

However, if selecting a big capacitor for VCC pin, it takes longer time to start up.

In such a case, a circuit shown in Fig.18 is effective for both purposes.

The startup time can be shortened by setting C1 smaller than C2. The hold time of VCC pin voltage is also made longer even at the sudden change of the load because the current is provided through C2 after startup.

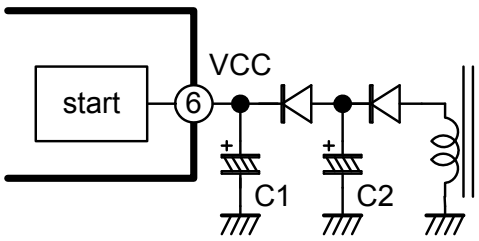


Fig.18 VCC circuit

(3) Gate drive circuit

Generally a resistor is connected between MOS gate pin and OUT pin of the IC in order to adjust switching speed and protect the vibration of the gate pin.

At that time, in some cases, the driving current that turns on a MOSFET and the driving current that turns off a MOSFET are required to be fixed independently.

In such case, connect a gate drive circuit shown in Fig.19 or Fig.20 between MOS gate pin and OUT pin of the IC.

In case of Fig.19, the current is restricted by R1+R2 at ON time and by only R2 at OFF time.

In case of Fig.20, the current is restricted only by R1 at ON time and by R1 and R2 connected in parallel at OFF time.

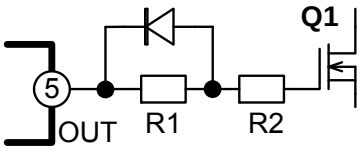


Fig.19 Gate drive circuit (1)

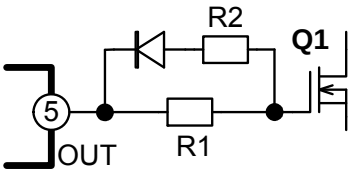


Fig.20 Gate drive circuit (2)

(4) LAT pin

・<u>In case of implementing overheat protection using NTC thermistor.</u>

Connecting thermistor TH1 to LAT pin, overheat protection (latch shutdown) can be realized as shown in Fig.15.

As LAT pin source current is 60uA (min.), select thermistor TH1 which resistance Rth fulfills the following equation at the temperature where overheat protection shall operate.

$$Rth@LAT \leqq 1.00V / 60uA \fallingdotseq 16.7k\Omega$$

・<u>In case of implementing latch shutdown by using an independent abnormal detection signal</u>

Connect NPN transistor Tr1 to LAT pin and input a detection signal to the base of Tr1 as shown in Fig.21.

Match the polarity in order that an input signal turns to High level in abnormal condition.

In addition no circuit is necessary that clamps LAT pin voltage more than latch shutdown threshold voltage at the steady state because the constant current flows out from LAT pin.

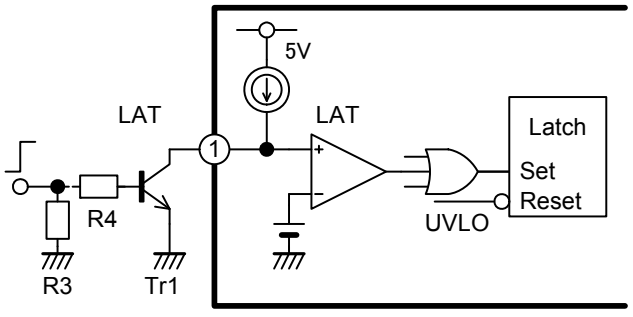


Fig.21 Latch shutdown function by an external signal

(5) Feedback & overload protection delay time

Circuit diagram of FB pin block is shown in Fig.22.

・Feedback circuit

A photo-coupler PC is connected as a feedback circuit that monitors the output voltage and performs PWM control.

This signal gives the threshold voltage for the comparator. Therefore if noise is added on to this signal, the output pulses lead to get out of order.

Usually a capacitor C3 is connected to protect noise.

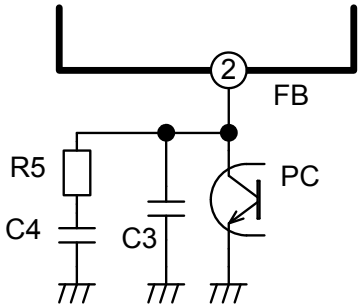


Fig.22 FB pin circuit composition

・Overload protection delay time

A time constant setting circuit is connected to FB pin that is composed R5 and C4 as shown in Fig.22 in addition to a feedback circuit in order to set the detection delay time of overload protection function.

Resistor R5 is connected so that C4 does not influence a feedback loop. It is approximately 20kΩ.

Capacitor C4 is a timing capacitor for the OLP oscillator after PC turns OFF by overload state.

A time constant obtained by charging and discharging C4 with a constant current is oscillating cycle of FB pin in period1 and period2 of overload protection operation time chart shown in Fig.23.

The overload protection delay time is calculated roughly as follows.

Tolp_delay[s] = 0.91 x C4 [uF]

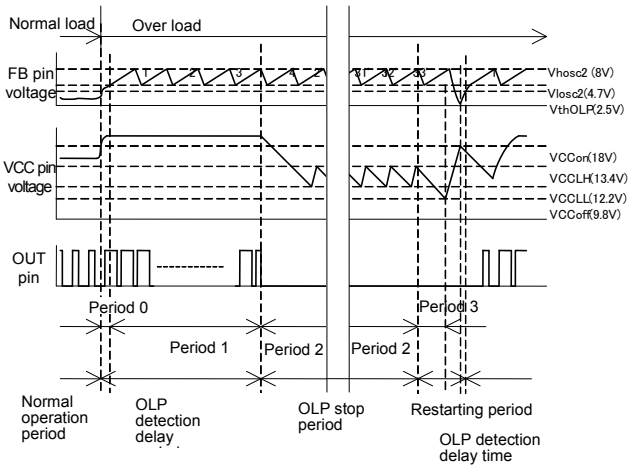
Similarly the shutdown time of FA5553/66 auto restart function is as follows.

Tolp_AutoRestart[s] = 6 x C4[uF]

Be careful that the times shown as period0 and period3 in Fig.23 are needed in addition to Tolp*** time described above.

In case of FA5554/66 auto restart type, if capacitor C4 is too small, VCC pin voltage falls and may be shutdown by UVLO before delay time elapses and shutdown state is caused by overload.

In this condition, the operation of repetition cycle by UVLO is executed not by repetition of switching/stop by auto restart function of overload.



Fig,23 Overload protection operation timing chart

(6) Current sense

As described in 8-(4) one shot circuit at page 16, the minimum ON width is set for FA5553/54/66/67. Consequently, it's relatively difficult to cause malfunction by surge current at the turn-on of power MOSFET.

However, if the surge current is too big at the turn-on or external noise other than turn-on is impressed, malfunction may be caused.

In such a case, add CR filter C6 and R7 to IS pin as shown in Fig.24.

In addition capacitor C6 must be placed nearest of the IC to operate more effectively and also wiring layout must be taken account.

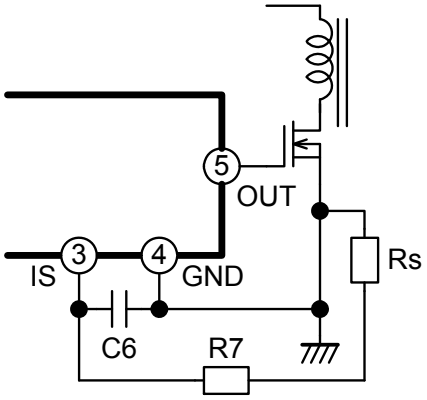


Fig.24 Filter of IS pin

(7) Improvement of input power at light load

FA5553/54/66/67 has function in it that reduces standby power consumption by lowering oscillation frequency at light load.

However, as the load condition differs according to the power supply set, the built-in setting of the IC may be insufficient to reduce standby power consumption.

In such a case resistor R8 must be connected as shown in Fig.25.

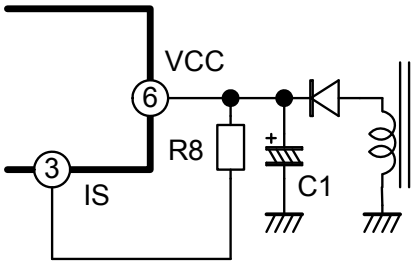


Fig.25 Compensation circuit for input power improvement at light load

(8) Reduction of input voltage dependency for overload detection level

When using overload protection function, as the gradient of the inductance current of a transformer differs according to input voltage, the current value that causes overload differs. It is possible to reduce input voltage dependency for overload detection level to connect resistor R9 between the auxiliary coil and IS pin as shown in Fig.26.

(9) Malfunction protection from minus potential of the pin

If minus high voltage is impressed to each pin of the IC, a parasitic device or element in the IC works and may cause malfunction.

Be sure that he voltage impressed to each pin must be within absolute maximum rating.

(10) Loss calculation

To use the IC within the rating, it is also necessary to calculate the loss of the IC. However, it is difficult to measure the loss directly.

Here an example of rough calculation of the loss is shown.

The total loss Pd of the IC is roughly calculated in the following equation.

Pd□VCC x (ICCop1 + Qg x fsw) + VVH x IHrun

Where VVh is the voltage impressed to VH pin, IHrun is the current flowing into VH pin in operation, VCC is the voltage of power supply, ICCop1 is current consumption of the IC, Qg is the gate input electric charge amount of MOSFET and fsw is switching frequency.

The rough value of total loss Pd is obtained by this equation and it is a little greater than practical loss.

In addition, as each attributes has its variation and temperature characteristics, these factors must be fully taken account.

Example)

If VH pin is connected to half-wave rectifier in case of AC 100V input, the average voltage impressed to VH pin is about 45V.

Moreover assuming that FA5553 is used under the condition, Tj=25℃, VCC=18V and Qg=80nC, each value is as follows according to this application manual.

IHrun=35uA (typ.)

ICCop1=1.35mA (typ.)

fsw=60kHz (typ.)

Then the loss of the IC with standard characteristics of the IC is calculated as follows.

Pd≒18V ∗ (1.35mA + 80nC ∗ 60kHz) + 45V ∗ 35uA

≒ 109 mW

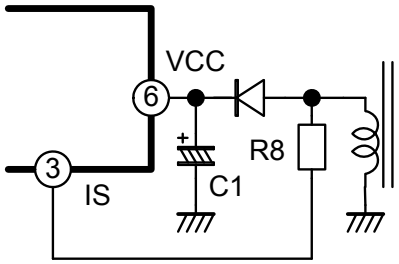
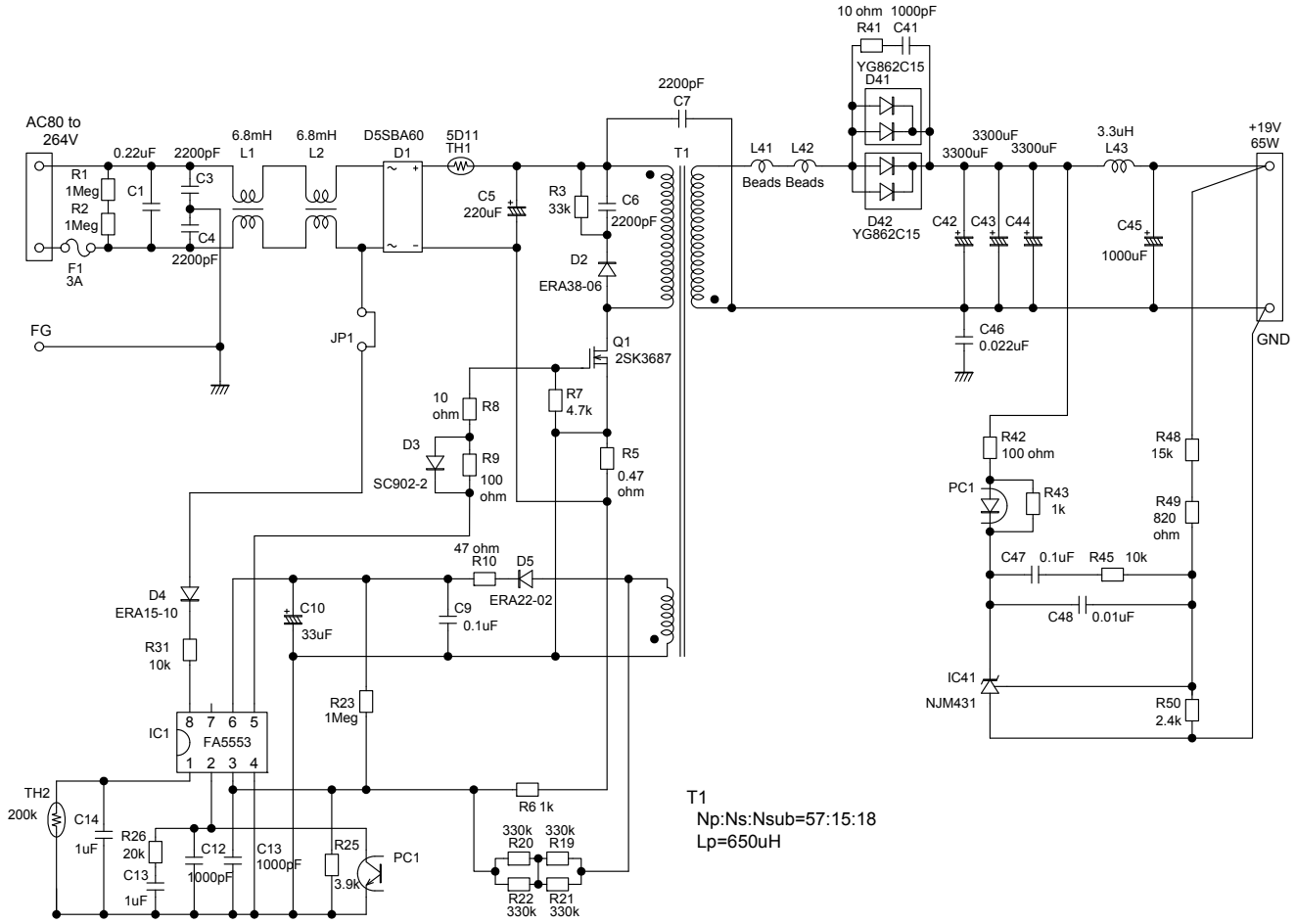


Fig.26 Reduction of input voltage dependency of overload detection level

10. Application circuit example



Note)

This application circuit example shows typical directions for use of this IC for reference and does not guarantee the operation and characteristics.