Combo-IC for Critical Conduction Mode PFC and Current Resonance

FA5560M

Application Note

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Caution)

- The contents of this note will subject to change without notice due to improvement.
- The application examples or the components constants in this note are shown to help your design, and variation of components and service conditions are not taken into account. In using these components, a design with due consideration for these conditions shall be conducted.

1. Outline

This IC combines the IC for critical conduction mode PFC and the highly effective and low-noise IC for current resonance. Although the start/stop sequence circuit, start-up circuit and standby circuit have been externally fitted conventionally, FA5560 has these circuits built-in, substantially reducing the number of parts and the system cost and saving the space for a power supply substrate.

2. Features

(1) Combined power supply IC controlling the critical conduction mode PFC and the current resonance
(2) Built-in start-up circuit capable of withstanding 500V
(3) Built-in standby function
(4) Built-in start/stop sequence
(5) Built-in protective function against brownout
(6) 20-pin SOP package

3. Outline drawing

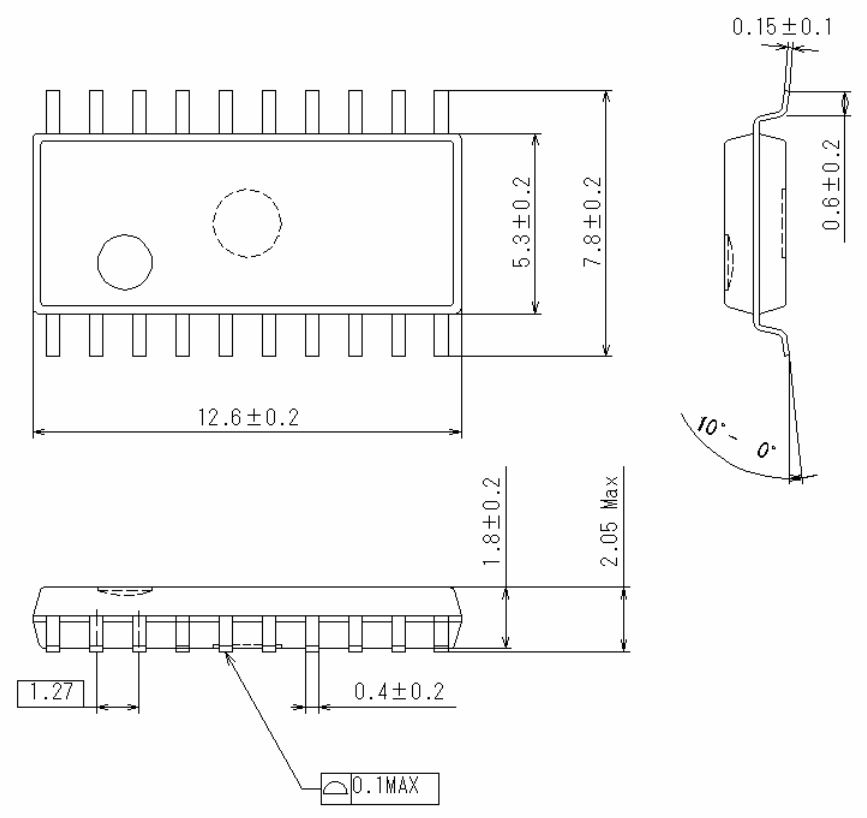

Fig.1 Package Dimensions

4. Block diagram

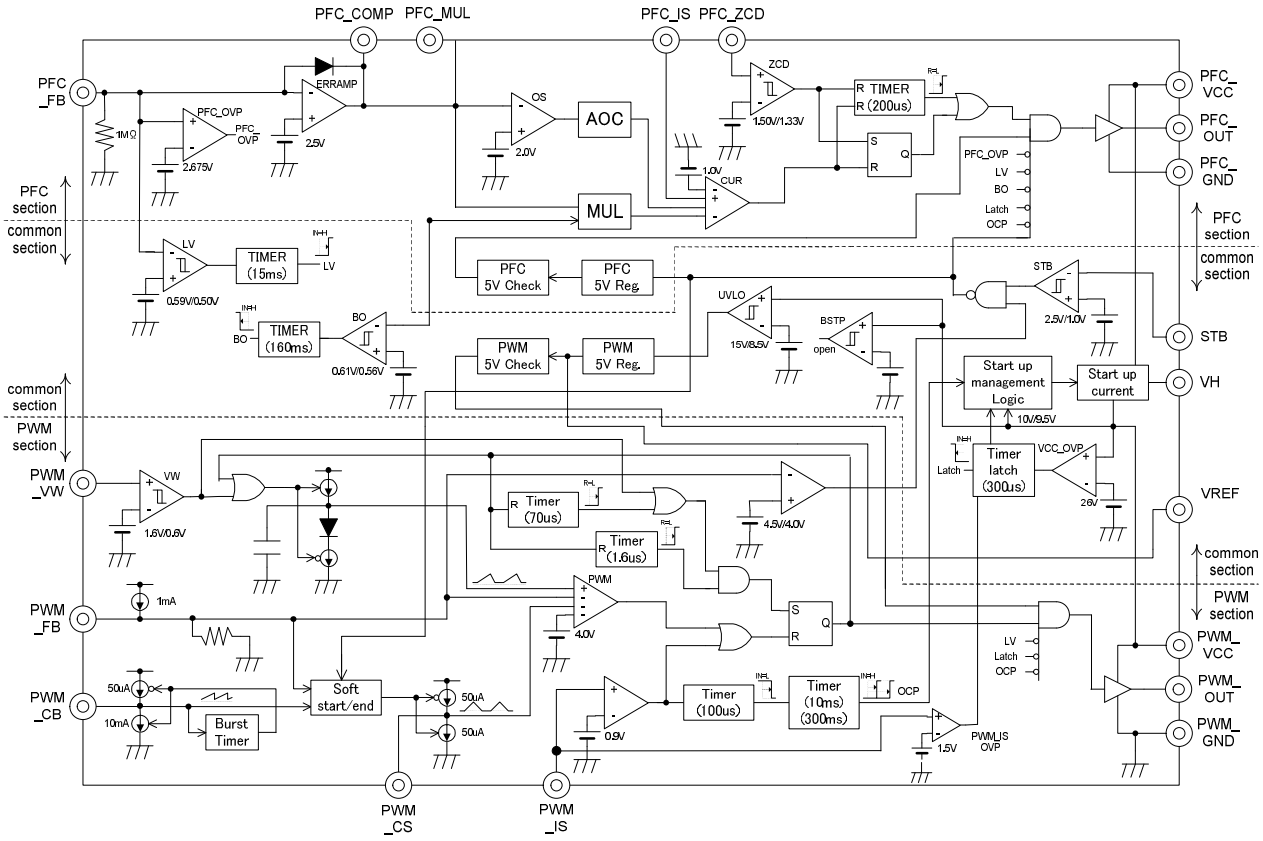

Fig.2 Basic Circuit Configuration

5. Terminal layout and function

端子番号 Terminal No.	端子記号 symbol	端子機能 Description	
1	VH	高電圧入力	High voltage input
2	(NC)	不使用	No connected
3	PFC_VCC	電源端子（PFC）	Power supply (PFC)
4	PFC_OUT	出力（PFC）	Output (PFC)
5	PFC_GND	グランド（PFC）	Ground (PFC)
6	PFC_ZCD	ゼロ電流検出入力（PFC）	Zero current detection (PFC)
7	PFC_IS	電流センス入力（PFC）	Current sense (PFC)
8	PFC_MUL	乗算器入力（PFC）	Multiplier input (PFC)
9	PFC_COMP	誤差アンプ補償用端子（PFC）	Compensation (PFC)
10	PFC_FB	フィードバック入力（PFC）	Voltage feedback input (PFC)
11	VREF	内部電源端子	Reference voltage output
12	STB	スタンバイ入力	Stand-by input
13	PWM_CB	バースト周期端子（PWM）	Burst operation (PWM)
14	PWM_CS	ソフトスタート／エンド端子（PWM）	Soft start/end (PWM)
15	PWM_FB	フィードバック入力（PWM）	Voltage feedback input (PWM)
16	PWM_IS	電流センス入力（PWM）	Current sense (PWM)
17	PWM_VW	巻線電圧検出入力（PWM）	Winding voltage detector (PWM)
18	PWM_GND	グランド（PWM）	Ground (PWM)
19	PWM_OUT	出力（PWM）	Output (PWM)
20	PWM_VCC	電源端子（PWM）	Power supply (PWM)

6. Outline of PFC unit

The PFC unit operates in the critical current mode. Outline of operation is described in two sections: “Switching operation” and “Operation for power factor improvement”.

6.1 Switching operation

Not using an oscillator, this IC performs switching operation in the critical mode applying self-oscillation. Fig. 3 shows the outlined waveforms of switching operation in the respective sections in the steady state.

t1. When Q_{PFC} is turned on, current of inductor L_1 increases from zero.

t2. When this current reaches the standard of current comparator (CUR.comp.) decided by output of the multiplier (MUL), the reset signal enters the R-S flip flop and Q_{PFC} turns off. When G_{PFC} turns off, the L1 voltage is inverted and, while supplying current to the output side through D1, the L1 current decreases. Meanwhile, voltage of the auxiliary winding is also inverted and plus voltage is generated.

t3. When the L1 current returns to zero completely, the L1 voltage resonates with the parasitic capacitor in the circuit and decreases rapidly. The voltage Vsub of the auxiliary winding installed in L1 also decreases at the same time.

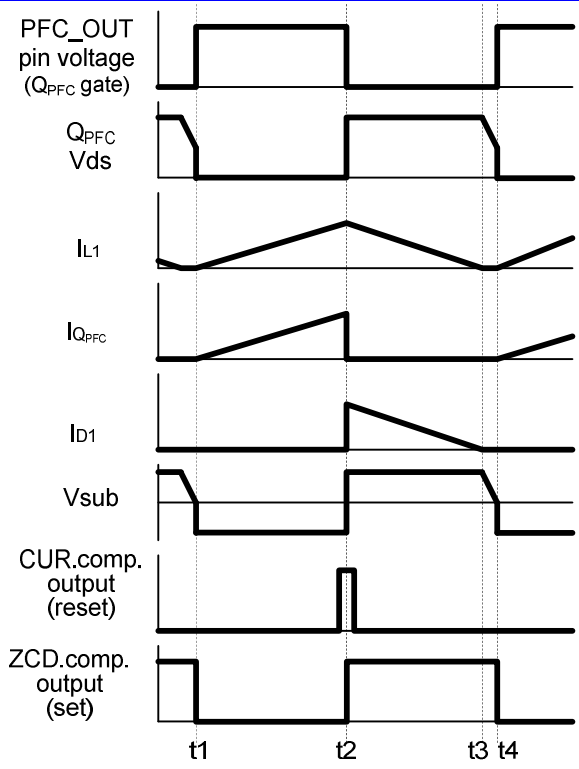

Fig.3 Timing chart switching operation

t4. When this Vsub decreases to the interior reference voltage of 1.33V, output of the zero current detector (ZCD.comp) is inverted. The set signal is input into the R-S flip flop because of this output fall, G_{PFC} is turned on again and the cycle moves to the next switching cycle (returns to t1).

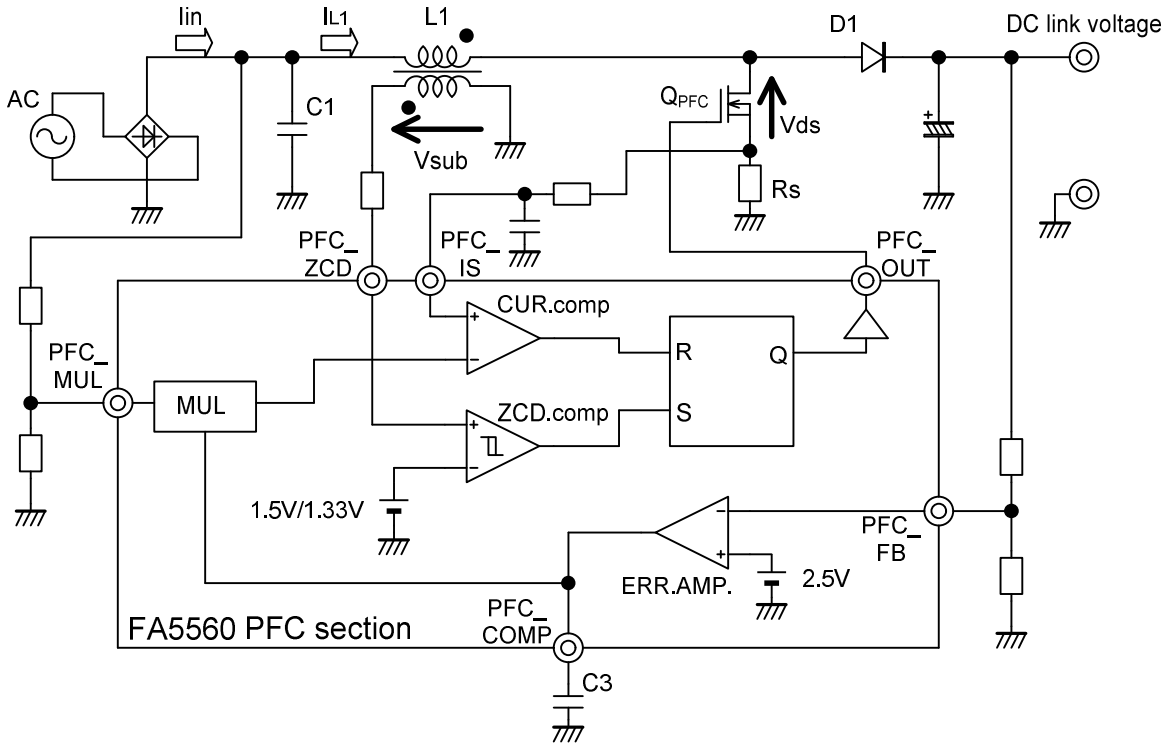

Fig.4 Block Diagram of PFC Converter

6.2 Operation of power factor improvement

As described in the section of switching operation, the current flowing in the inductor is repetition of triangular waves. The mean value ($I_{L1(mean)}$) of these continuous triangular waves is 1/2 of the peak value ($_{IL1(peak)}$). Therefore, the current flowing from AC power supply can be made into a sinusoidal wave when the peak value of the inductor current is controlled into a sinusoidal wave state and ripple current in switching is removed. In an actual circuit, the multiplier (MUL) within the IC is used to make the peak value of the inductor current to be a sinusoidal wave state.

Voltage of the COMP terminal, which becomes output of the error amplifier (ERRAMP), becomes almost DC voltage in a steady state due to C3. This voltage is input into the multiplier. The waveform of the rectified AC input voltage is entered in another input into the multiplier. As a result, a waveform of sinusoidal wave state proportionate to the AC input voltage, which is the product of these two waveforms, is output from the multiplier.

This output voltage waveform of sinusoidal wave state is input into the current comparator (CUR.comp) as the standard of inductor current. As a result, the peak value (IL1(peak)) of the inductor current becomes continuous triangular waves in a sinusoidal wave state. By removing the switching ripples of this inductor L1's current and averaging them by C1, the current flowing form the AC input voltage becomes almost like a sinusoidal wave and thus power factor can be improved.

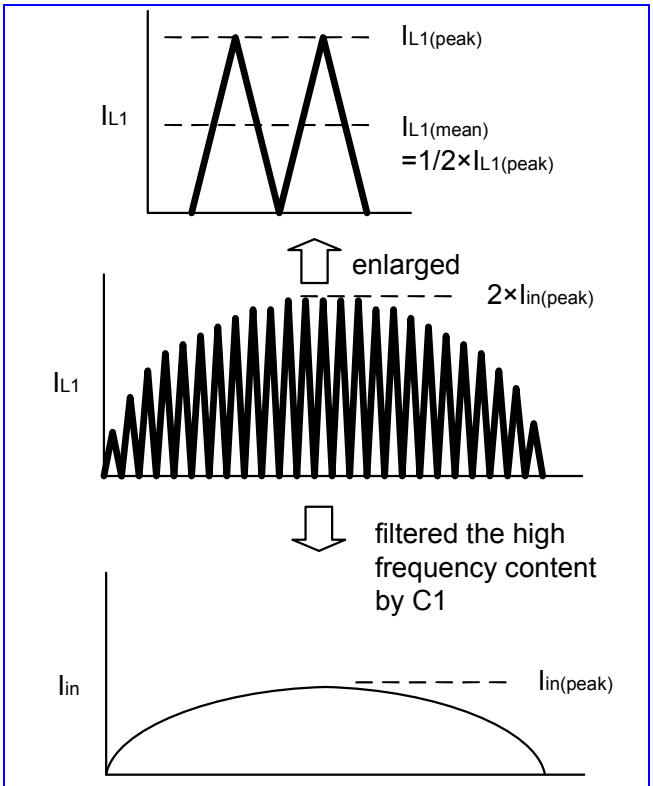

Fig.5 Outline of inductor and AC input current

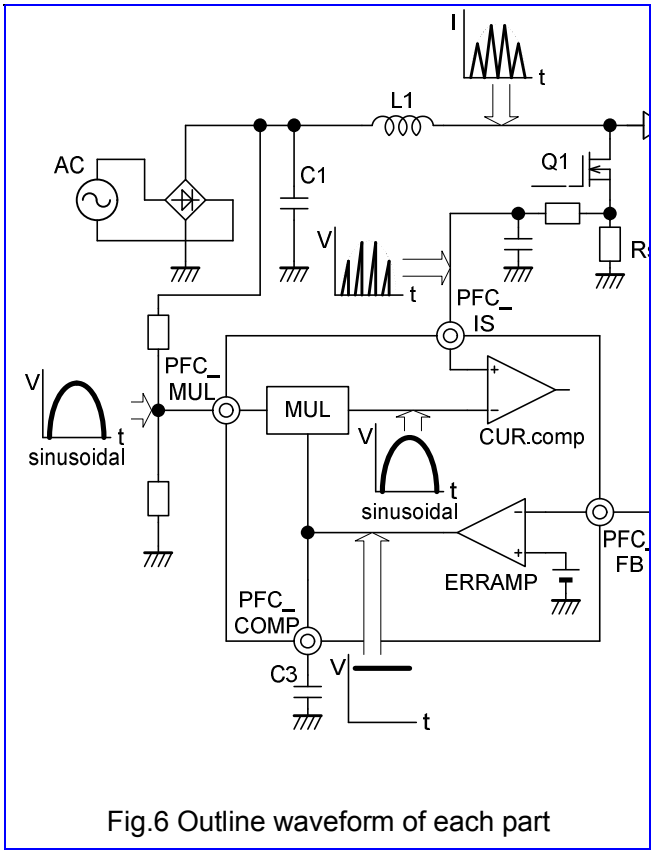

Fig.6 Outline waveform of each part

7. Description of PFC block

7.1 Error amplifier

Fig. 7 shows the circuit around the error amplifier. This amplifier controls the DC intermediate voltage, which is the output of the converter for power-factor improvement, to keep it at a certain level, and this IC uses a transconductance amplifier. It handles the voltage as input signal and the current as output signal.

The non-inverting input terminal is connected to the interior reference voltage of 2.5V(typ.) within the IC. It is the terminal to input the DC intermediate voltage, and usually this voltage is input after resistor voltage division.

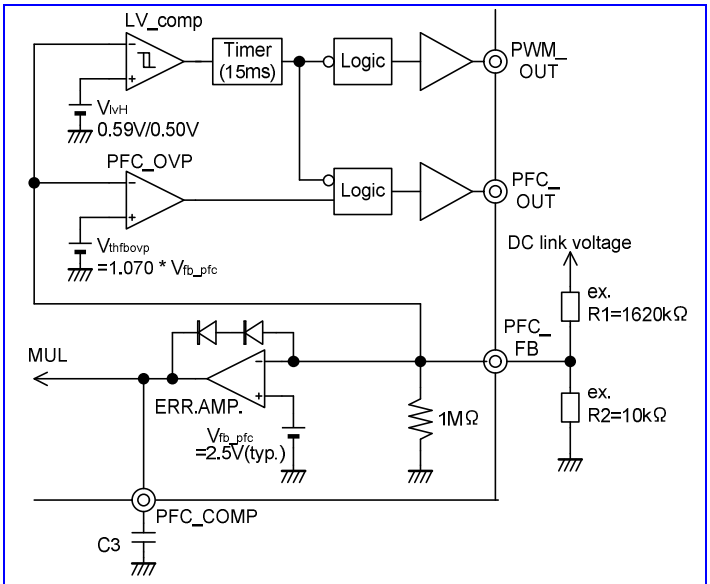

Fig.7 Error amplifier circuit

For inverting input, a 1MΩ resistor for detection of PFC_FB short is connect. Output of the error amplifier is connected to the multiplier. Usually the output voltage range of 2.04V to 3.54V(typ.) is used. In addition, a diode is connected between the error amplifier's input and output to prevent its output voltage from dropping excessively in a transient situation such as sudden change of load.

Usually the DC intermediate voltage includes many ripples of frequency twice that (generally 50 or 60Hz) of an AC line. If the ripple components equivalent to twice the frequency of an AC line appears in the error amplifier's output in a large quantity, the converter for power-factor improvement does not operate stably. Therefore, usually a capacitor is connected between the PFC_COMP terminal, which is the error amplifier's output, and the PFC_GND terminal to set the cutoff frequency to about 20Hz so that the ripple components do not appear in the error amplifier's output.

7.2 Overvoltage protection

This is the circuit to restrict voltage when the DC intermediate voltage exceeds the preset value. When the converter is started or the load changes suddenly, in some cases the DC intermediate voltage may increases higher than the preset value. In such a case, this circuit restricts increase of it and protects the other circuits. As shown in Fig. 7, the circuit for overvoltage protection consists of the comparator (PFC_OVP) and the reference voltage. This reference voltage is set to 1.070 times that of error amplifier. Usually voltage of the PFC_FB terminal operates at 2.5V almost same as that of the error amplifier. If the DC intermediate voltage increases for some reason and the FB terminal's voltage exceeds the comparator's reference voltage, the output voltage of the comparator (PFC_OVP) is inverted during that time and the PFC_OUT pulse is stopped. When the

DC intermediate voltage is returned to the normal, the PFC_OUT pulse is output again.

7.3 Detection of FB short

For example, in the circuit shown in Fig. 8, if voltage is not input into the PFC_FB terminal due to a short failure of R2 in the resistance voltage division circuit or a open failure of R1, the error amplifier cannot control the constant voltage and the DC intermediate voltage increases extraordinarily. In addition in this case, the overvoltage protection circuit cannot operate because detection of the DC intermediate voltage is abnormal. This IC contains a PFC_FB short detection circuit to avoid such a situation. This circuit consists of the reference voltage of 0.50 (typ.), comparator (LV) and dealy timer. If input voltage of the FB terminal decreases to 0.50V or lower due to a short failure of R2 or an open failure of R1, output of the comparator (LV_comp) is inverted and output of both PFC_OUT and PWM_PUT is stopped after the timer set time of 15ms passes.

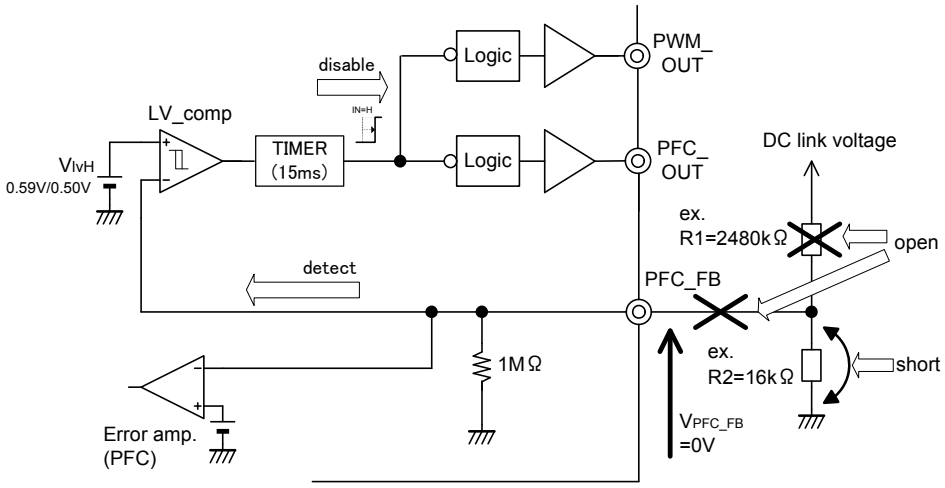

Fig.8 Open/Short protection of PFC_FB pin

If an open failure occurs between the PFC_FB terminal and the resistance voltage division circuit, the PFC_FB terminal voltage is forcibly lowered by the 1MΩ constant current source connected to the PFC_FB terminal within the IC and the circuit is stopped likewise. If voltage of the PFC_FB terminal drops almost to zero once and the voltage returns to the normal after the IC's output is stopped, pulse of PFC_OUT and PWM_OUT is output again.

7.4 Multiplier

The multiplier is the circuit to control the input voltage to keep it in a sinusoidal wave. One input is connected to the PFC-MUL terminal and inputs the voltage rectified from the AC input voltage after voltage division. Another input is connected to the error amplifier's output within the IC. Usually output of the error amplifier is almost DC, and a sinusoidal voltage, the amplitude of which changes according to the error amplifier's output voltage, is output from the multiplier. This multiplier's output becomes the standard for the current comparator and controls the input voltage to keep it in a sinusoidal wave.

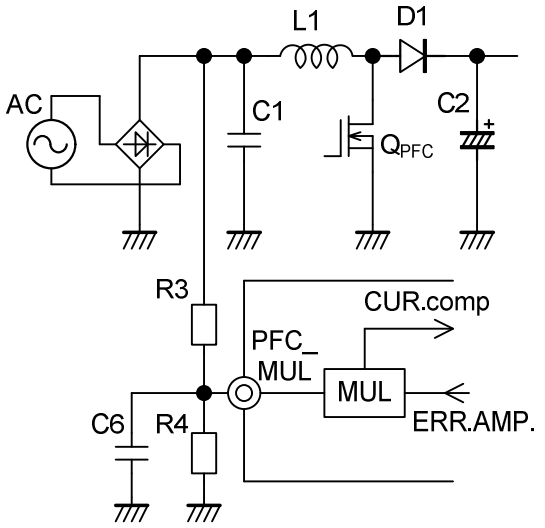

Fig.9 Multiplier circuit

Taking the multiplier's dynamic range into account, the peak voltage, which is input into the PFC_MUL terminal, is usually used in the range of 2.5V or lower. The voltage after rectification of the AC input voltage contains a lot of noises caused by switching of Q_{PFC}. Usually the capacitor C6 for filtering is connected to eliminate influence of these noises.

7.5 Current sensing comparator

One input is connected to the multiplier's output, which becomes the standard for current, within the IC. Another input is connected to the PFC_IS terminal, converts the source current of MOSFET to the voltage by the detecting resistor Rs and inputs it. In each switching cycle, when the current of MOSFET reaches the standard value decided by the multiplier's output, output of the current comparator is inverted and gives the reset signal to the RS flip flop. As a result, MOSFET is turned off and the "On state" of MOSFET for that cycle is finished. In addition, the upper limit for the reference voltage of the current comparator is limited to 1.1V (max.) within the IC.

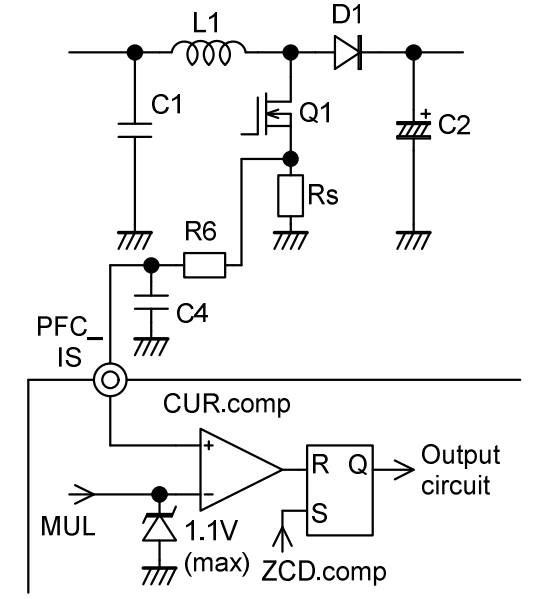

Fig.10 Current sense comparator circuit

Therefore, in such a transient situation as when the converter is started or input voltage and load change suddenly, the max value of the MOSFET's current is limited to the value decided by the following formula. Usually the CR filter is connected between the PFC_IS terminal and the sensing resistor Rs to prevent a malfunction caused by noises. $Id(\max) = \frac{1.1}{Rs}$

7.6 Zero current detector circuit

This IC performs switching operation in the critical mode applying self-oscillation, not the fixed frequency sent by an oscillator. The zero current detector is the circuit detecting that the inductor's current is zero to perform the critical mode operation.

Voltage of the auxiliary winding installed on the inductor is input into the ZCD terminal in the polarity shown in Fig. 11. Then plus voltage is generated in this winding while MOSFET is off. Subsequently when the inductor current returns to zero, voltage of the auxiliary winding decreases rapidly.

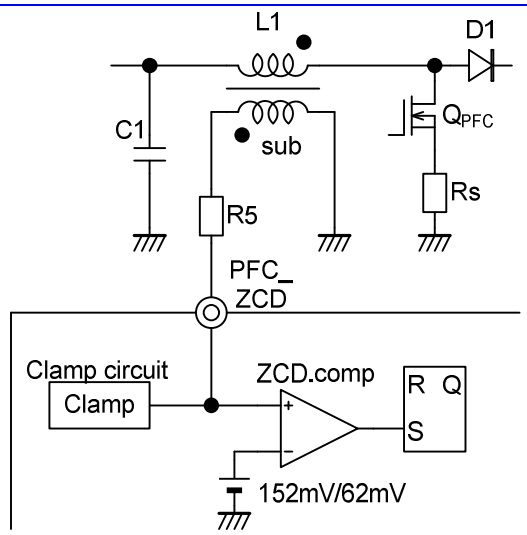

Fig.11 Zero current detector circuit

This voltage drop is detected by ZCD.comp, the set signal is sent to the RS flip flop and MOSFET is turned on to move to the next cycle.

Voltage of the auxiliary winding changes significantly depending on circuits and input voltage. Therefore a clamp circuit for upper limit of 9.2V (typ.) and lower limit of –0.83V (typ.) is provided to cope with this problem. A resistor for limiting of current is inserted between the auxiliary winding and it according to the current rating of the clamp circuit and such.

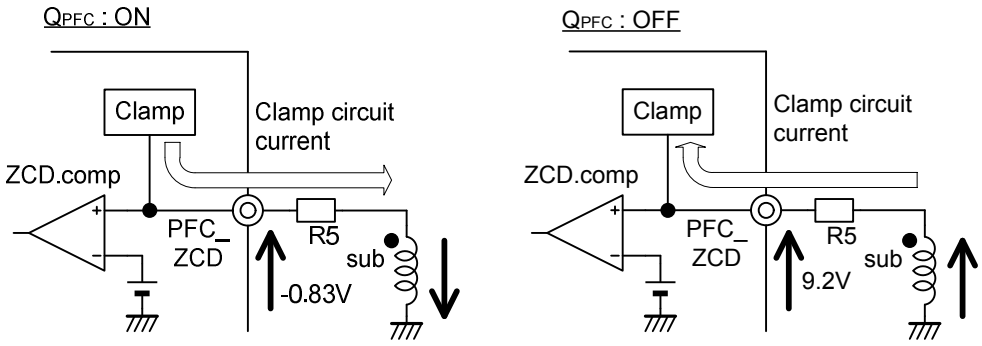

Fig.12 Clamp circuit of PFC_ZCD pin

Limit the clamp circuit' current to 3mA or lower to operate the IC normally. On the other hand, if the current that is flowed to the clamp circuit is too small, it may not operate stably. Therefore the resistor R5 for limiting of current should be 47kΩ or lower. Minus voltage is generated in the auxiliary winding while MOSFET is on. Then current flows out from the clamp circuit, and voltage of the PFC_ZCD terminal is clamped to –0.83V (typ.). Plus voltage is generated in the auxiliary winding while MOSFET is off. Then current flows into the clamp circuit and clamps the voltage of PFC_ZCD terminal to 9.2V (typ.).

7.7 Correcting circuit for light load

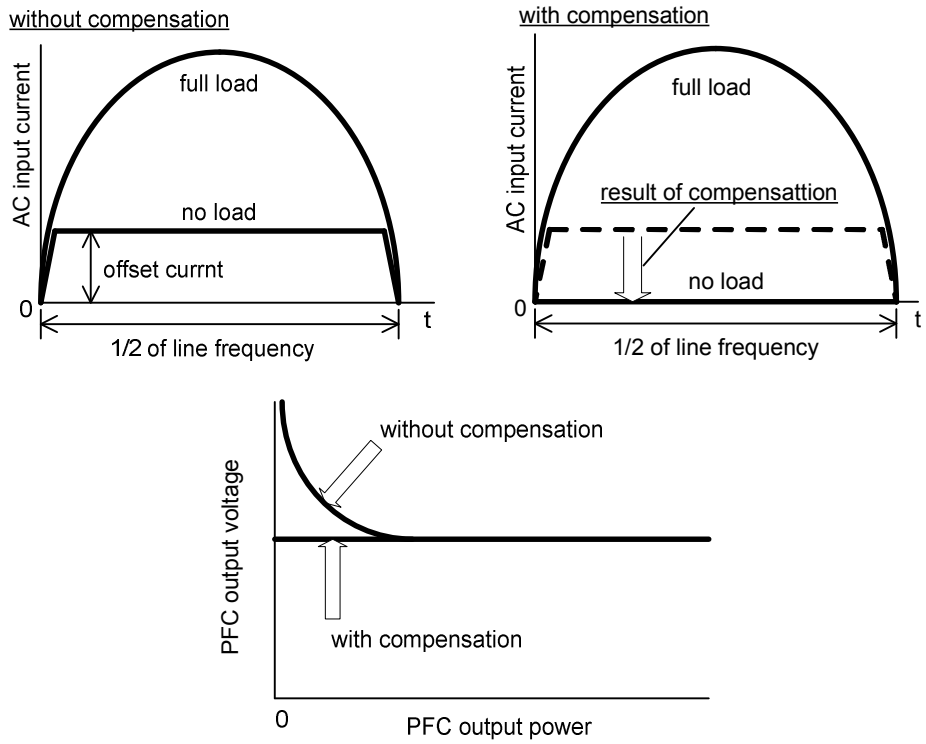

Fig.13 Outline of operation when multiplier has a positive offset

If there is no offset voltage in output of the multiplier that gives the reference value to the current comparator, the input voltage to the converter becomes almost zero when the load of the power-factor improving converter becomes complete no-load. Actually in some cases, however, offset voltage may be generated due to variation in ICs. If this offset voltage is plus, input current equivalent to it flows into the converter even in the status of no or light load. In this case, the DC intermediate current increases extraordinarily because the incoming current becomes excessive. The correcting circuit (AOC) for light load is provided to avoid such as a phenomenon.

Output voltage of the error amplifier is usually used at about 2V or higher. If this output voltage decreases to 2V or lower, the correcting circuit for light load operates. If there is a plus offset in the multiplier's output, output voltage of the error amplifier drops to 2V or lower when output of the power-factor improving converter becomes no or light load. Then the offset voltage is corrected by the correcting circuit for light load on the current comparator side. Due to this operation, the DC intermediate current does not increase extraordinarily and is always kept at a certain voltage even in the case of no or light load. In addition, stable operation can be performed because the correction amount changes in the linear manner according to output of the voltage error amplifier.

7.8 Restart timer

This IC uses self-oscillation that does not use an oscillator, and the signal from the zero-current detector turns on MOSFET in the steady state. However, some trigger signal is necessary when

generating the first “On” signal in starting or for stable operation in light load. This IC is also provided with a restart timer and generates a trigger signal automatically if output of the IC is off for 200μs or more continuously. This signal enables stable operation even in starting or light load.

7.9 Circuit for prevention of malfunction in low voltage

This IC incorporates a circuit for prevention of malfunction in low voltage. Operation is started at 15.0V (typ.) when the power-supply voltage increases from zero. Operation is stopped at 8.5V (typ.) when it decreases after operation is started. The circuit for prevention of malfunction in low voltage operates and the PFC_OUT and PWM_OUT terminals become low and the output is cut off while the IC is stopped.

7.10 Output circuit section

The output section is the push-pull circuit, enabling to drive MOSFET directly. The peak current of the output section is sink 10A max and source 0.5A max.

7.11 Protection for low AC input voltage (brownout)

The AC input voltage is monitored by the PFC_MUL terminal, and the peak voltage of AC input is detected. If the peak voltage of the PFC_MUL terminal decreases to lower than the threshold vale VthBO for the time set by the brownout timer, the output pulse of PFC and PWM is stopped. If the peak voltage of AC input reaches the threshold value of the brownout comparator or bigger, stop of PFC and PWM’s output pulse is released.

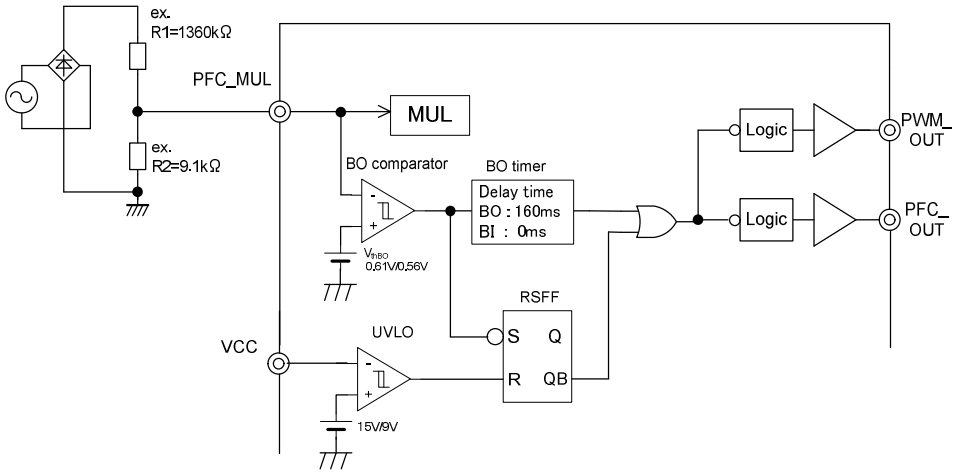

Fig.14 Brownout circuit

8. Operation of PWM section

8.1 Configuration of basic circuit

Fig. 15 shows the basic circuit configuration. The PWM section operates in the combined-oscillation current resonance mode. The low-side MOSFET (Q1) is the forced oscillation driven by a control IC, and the high-side MOSFET (Q2) is called the combined oscillation because it is the self-oscillation driven by the auxiliary winding P2 of the isolating transformer. Current resonance is performed by the leakage inductance of the isolating transformer and the series resonant circuit of the capacitor Cr.

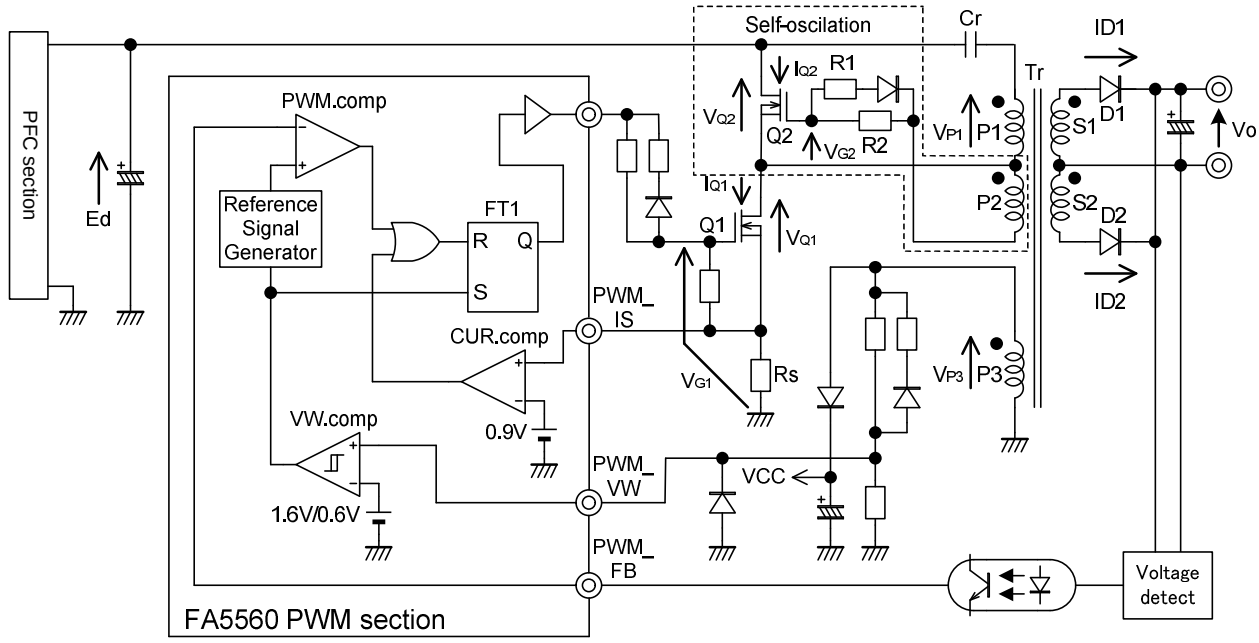

Fig.15 Basic Circuit Configuration of PWM section

8.2 Description of current resonance operation

The following describes the operation of the combined-oscillation current resonance circuit. The timing chart is shown in Fig. 16 and the current path during I to VI in Fig. 17.

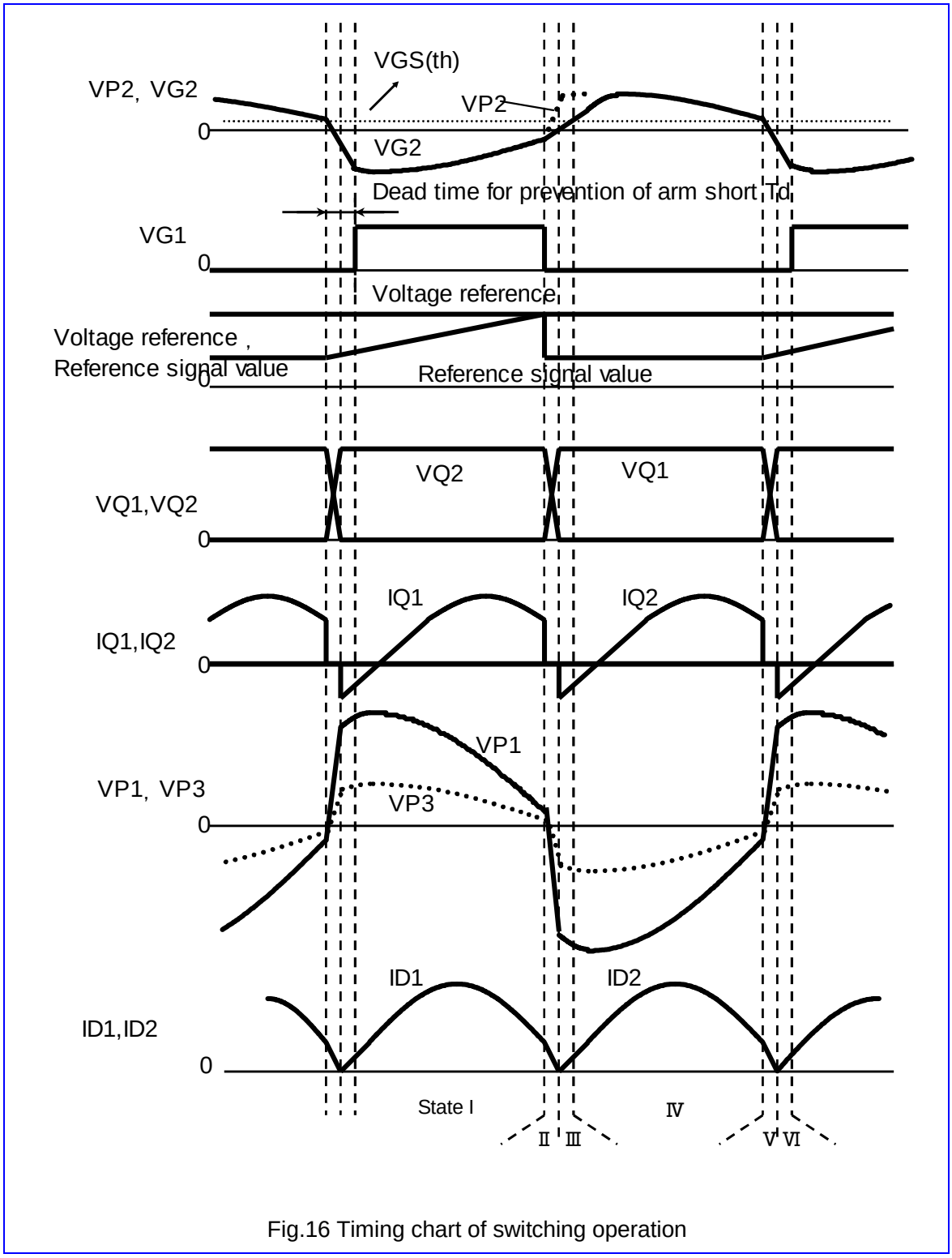

Fig.16 Timing chart of switching operation

Fig. 17 shows the current path during I to VI. In Fig. 17.1 to 17.6, capacitors Cq1 and Cq2 indicate the output capacity of Q1 and Q2 respectively, and diodes Dq1 and Dq2 indicate parasitic diodes Q1 and Q2. Lm stands for the exciting inductance of T1 and RI for the resistance. L1 is the inductance for the resonant current sent to the load of the secondary side and described temporarily in the circuit of Fig. 17 for the purpose of explaining this section.

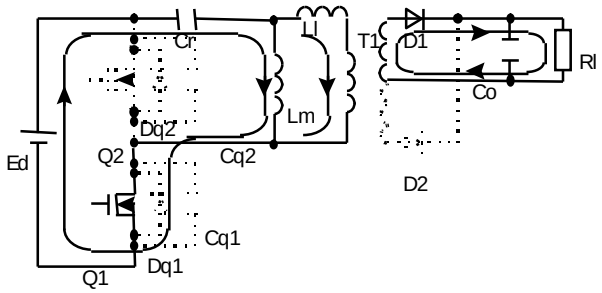

Fig.17.1 Current path at state I

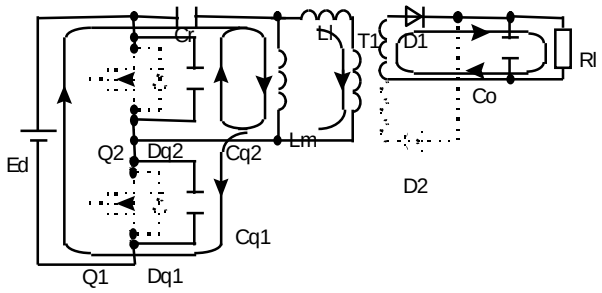

Fig.17.2 Current path at state II

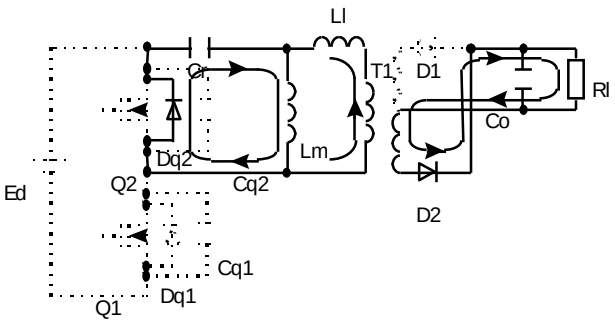

Fig.17.3 Current path at state III

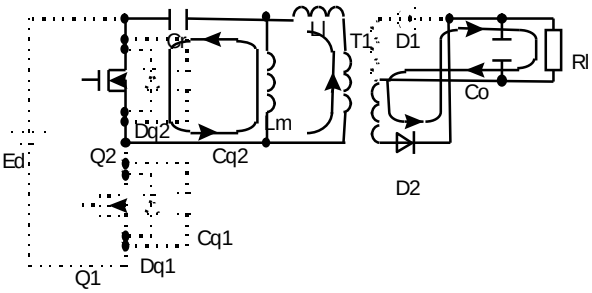

Fig.17.4 Current path at state IV

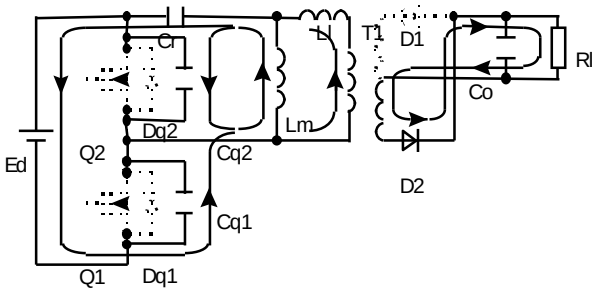

Fig.17.5 Current path at state V

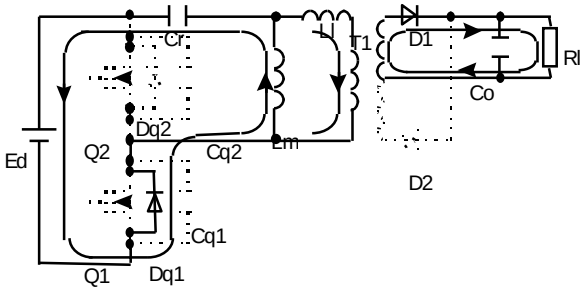

Fig.17.6 Current path at state VI

Fig. 17 Current Path during I to VI

State I (See fig. 17.1.)

If Q1 is on and Q2 is off and the current flows in the circuit as shown in a continuous line in the figure, the following formula (1) holds when the currents flowing in Cr, LI and Lm are represented as I_{Cr}, I_{LI} and I_{Lm} respectively:

$I_{Cr} = I_{LI} + I_{Lm}$ ..... (1)

In addition, from the product of A and T (ampere and turn), the formula (2) holds:

$N_{P1} \times I = N_{S1} \times I_{D1}$ ..... (2)

N_{P1}: Turns of winding P1, N_{S1}: Turns of winding S1, and I_{D1}: D1 current

Power is accumulated in LI and Lm while it is supplied to the load.

State II (See Fig. 17.2.)

If Q1 is turned off, Cq1 is charged by the energy stored in LI and Lm, and Cq2 is discharged. In this state, the above formulas (1) and (2) and the following formulas (3) and (4) hold.

$I_{Cr} = I_{Cq1} + I_{Cq2}$ ..... (3)

$I_{Cq1} = I_{Cq2}$ ..... (4)

I_{Cq1}: Cq1 current, I_{Cq2}: Cq2 current

Accordingly, voltage increase rate of Q1 is restricted by the charging speed of Cq1 and voltage decrease rate of Q2 by the discharging speed of Cq2.

State III (See Fig. 17.3.)

When the voltage of Cq1 reaches the DC intermediate voltage Ed and Cq2 becomes zero voltage, Dq2 is electrically continued and current flows in the path shown in the figure. Accordingly voltage of Q1 is clamped to Ed. In this state, the above formulas (1) and (2) hold and the following formula (5) holds.

$I_{Cr} = I_{Dq2}$ ..... (5)

I_{Dq2} : Dq2 current

By turning Q2 on while current is flowing in Dq2, ZVS (zero voltage switching) is achieved.

State IV (See Fig. 17.4.)

The current on the transformer's primary side is inverted and current flows in the path shown in figure. The above formulas (1) and (2) hold in this state too. Energy is stored in LI and Lm.

State V (See Fig. 17.5.)

Q2 is turned off, and by the energy stored in LI and Lm, Cq1 is discharged and Cq2 is charged. In this state too, the above formulas (1), (2), (3) and (4) hold. Accordingly the voltage decrease rate of Q1 is restricted by the discharge speed of Cq1 and the voltage increase rate of Q2 by the charging speed of Cq2.

Stage VI (See Fig. 17.6.)

When voltage of Cq1 becomes zero voltage and that of Cq2 reaches Ed, Dq1 is electrically continued. Therefore the voltage of Q2 is clamped to Ed. In this state, the above formulas (1) and (2) and the following formula (6) hold:

$I_{Cr} = I_{Dq1}$ ..... (6)

I_{Dq1}: Dq1 current

In addition, by turning Q1 on while current is flowing in Dq1, ZVS is achieved.

Namely, the I_{Lm} current circulates through the primary side, and it is supplied to the secondary side in the secondary reduced value of the I_{Lm} current.

9. Description of PWM block's operation

9.1 Circuit of Q1 pulse width control

Fig. 18 shows the timing chart for Q1 pulse width control.

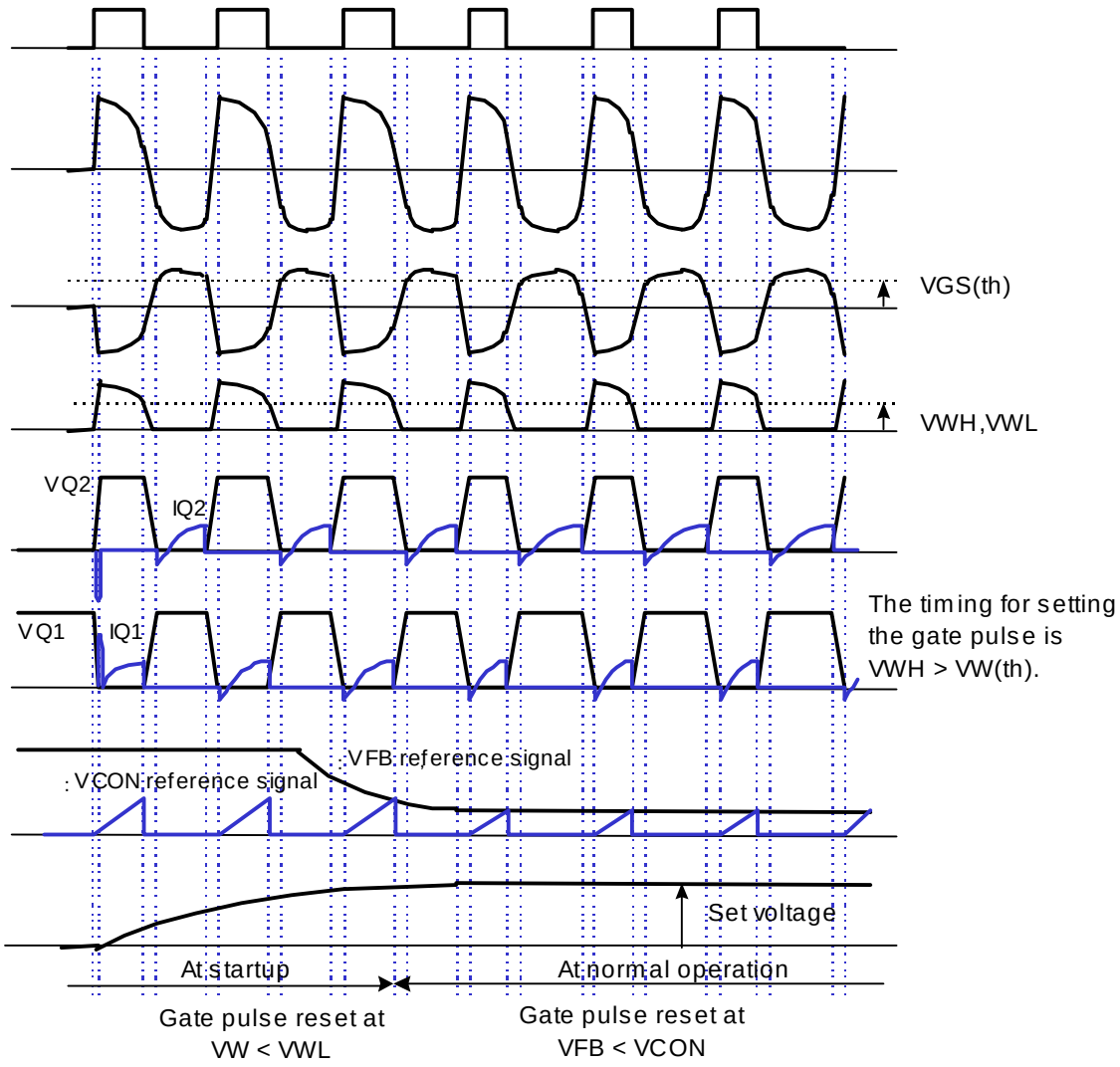

Fig.18 Q1 Pulse Width Control Timing Chart

The Q1 pulse width control circuit controls the output voltage Vo of the DC/DC converter's secondary side to keep it constant. The input signals into this circuit are the output signal VW of the polarity checking circuit for winding voltage and the voltage command value V_{PWM_FB} that controls the secondary side's output voltage to keep it constant.

In the circuit shown in Fig. 15, while Q2 is on, voltage of the auxiliary winding for the transformer's control power source (VCC) becomes negative and V_{PWN_VW} becomes zero level. When Q2 is turned off, voltage of the auxiliary winding is inverted to be positive and V_{PWM_VW} exceeds the threshold value V_{thvw2}.

The timing for Q1 turning on is given in this timing. In addition, adjustment of time constant for the capacitor of the PWM_VW terminal is necessary so that gate signal is output after voltage of Q1 becomes zero.

For creation of the voltage command value (V_{PWM_FB}), the output-voltage adjustment circuit of the secondary side creates the error signal for the set value of output voltage, and the error signal is isolated by a photo coupler and converted into the collector voltage value of the photo-receiving side's transistor.

In steady time, the difference between this voltage command value V_{PWM_FB} and the reference signal V_{CON}, which increases in proportion to the time that passes from the timing when the auxiliary winding's voltage is inverted to be positive, is compared by the comparator PWM.comp, and in the timing when the reference signal value exceeds the voltage command value, the RS flip flop FT1 is reset and the timing for turning off Q1 is given. When Q1 is turned off, the gate voltage VG2 of Q2 is inverted form negative to positive, and when VG2 exceeds the gate threshold value VGS (th), Q2 is turned on. The reference signal V_{CON} is set to return to the initial value in the timing when V_{PWM_VW} becomes lower than Vthvw2 after Q1 is turned off.

In start-up, in some cases the transformer's winding voltage VP1 (See Fig. 15) may change from positive to negative before the reference signal exceeds the voltage command value after Q1 is turned on. In this case, to prevent arm short circuit, this IC has the function to forcibly turn off Q1 before the transformer's winding voltage VP1 changes form positive to negative, to be exact, in the timing when V_{PWM_VW} becomes lower than the threshold value V_{thvw1}.

9.2 Standby operation

During stand-by operation, the load operates at 1W or lower, very small power compared with the rated load. In this case, if switching is performed continuously just like at the rated load, power loss increases, deteriorating the conversion efficiency. If the STB terminal voltage is made to be Vstbon or lower, the IC enters a burst operation and reduces loss of the converter. Fig. 19 shows the timing chart for the stand-by mode. If the STB terminal (No.12) is made to be Vstboff or more, operation is performed in the usual continuous switching.

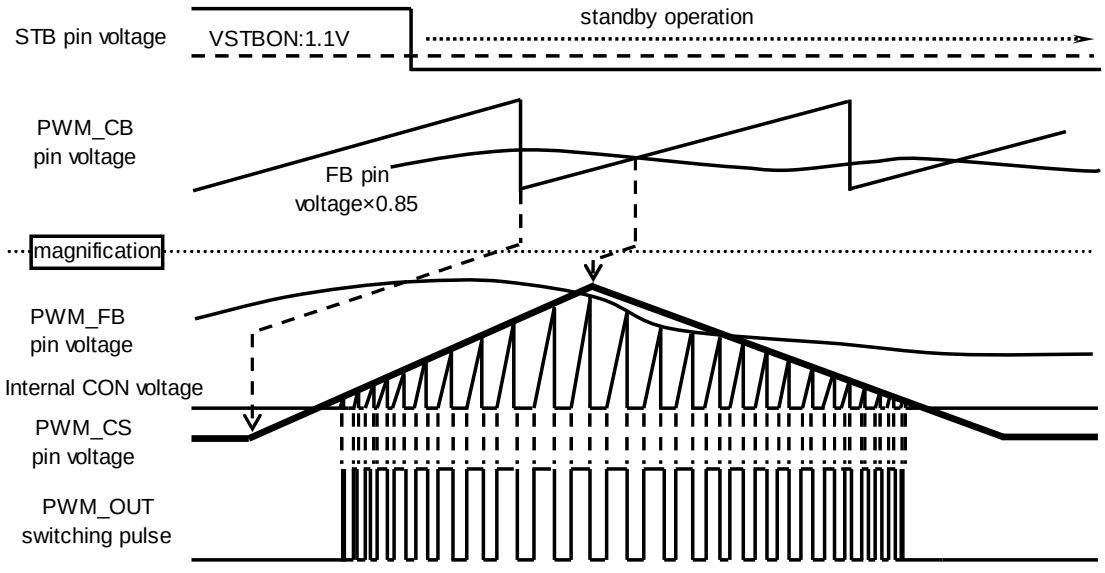

Fig.19 Timing chart (Stand-by mode)

9.3 Overcurrent protection

Each overcurrent protection operates pulse by pulse. Fig. 20 shows the timing chart for overcurrent. If the PWM_IS terminal voltage increases to the overcurrent protection threshold voltage Voc or over, output of the PWM_OUT terminal is stopped.

Continuous overcurrent protection operates in the automatic return mode. Fig. 21 shows the timing chart for overcurrent protection.

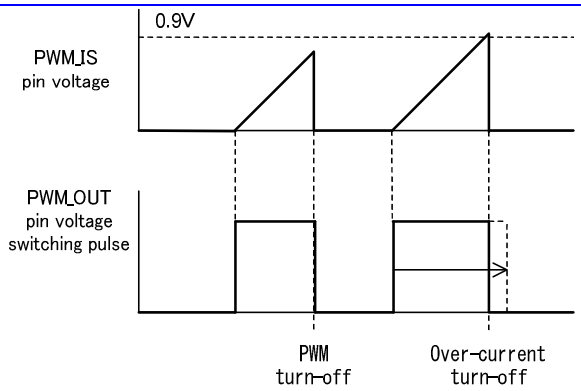

Fig.20 Timing chart from normal operation to over-current

State 1 If the IS terminal voltage exceeds the overcurrent detecting voltage of 0.9V, the OCP timer starts operation. The timer continues operation as far as the IS terminal voltage exceeds 0.9V again within 100μs.

State 2 If operation of the OCP timer continues for 10ms up to the forced stop, PWM_OUT of IC output stops. The VCC voltage decreases to the ON threshold value for the start-up circuit because it is supplied from the winding. The start-up circuit operates and the VCC voltage increases to the OFF threshold value for the start-up circuit. Then the start-up circuit stops and the VCC voltage decreases again.

State 3 If operation of the OCP timer continues for 300ms up to the restart operation, the start-up circuit stops and the VCC voltage decreases to the OFF threshold value of UVLO.

State 4 When the VCC voltage reaches the OFF threshold value of UVLO, the start-up circuit operates and the VCC voltage increases. The IC operates again when the VCC voltage reaches the ON threshold value of UVLO.

The power source repeats the states 1 to 4 unless the state of overcurrent is released. If it is released, the power source returns to the normal operation after the state 4.

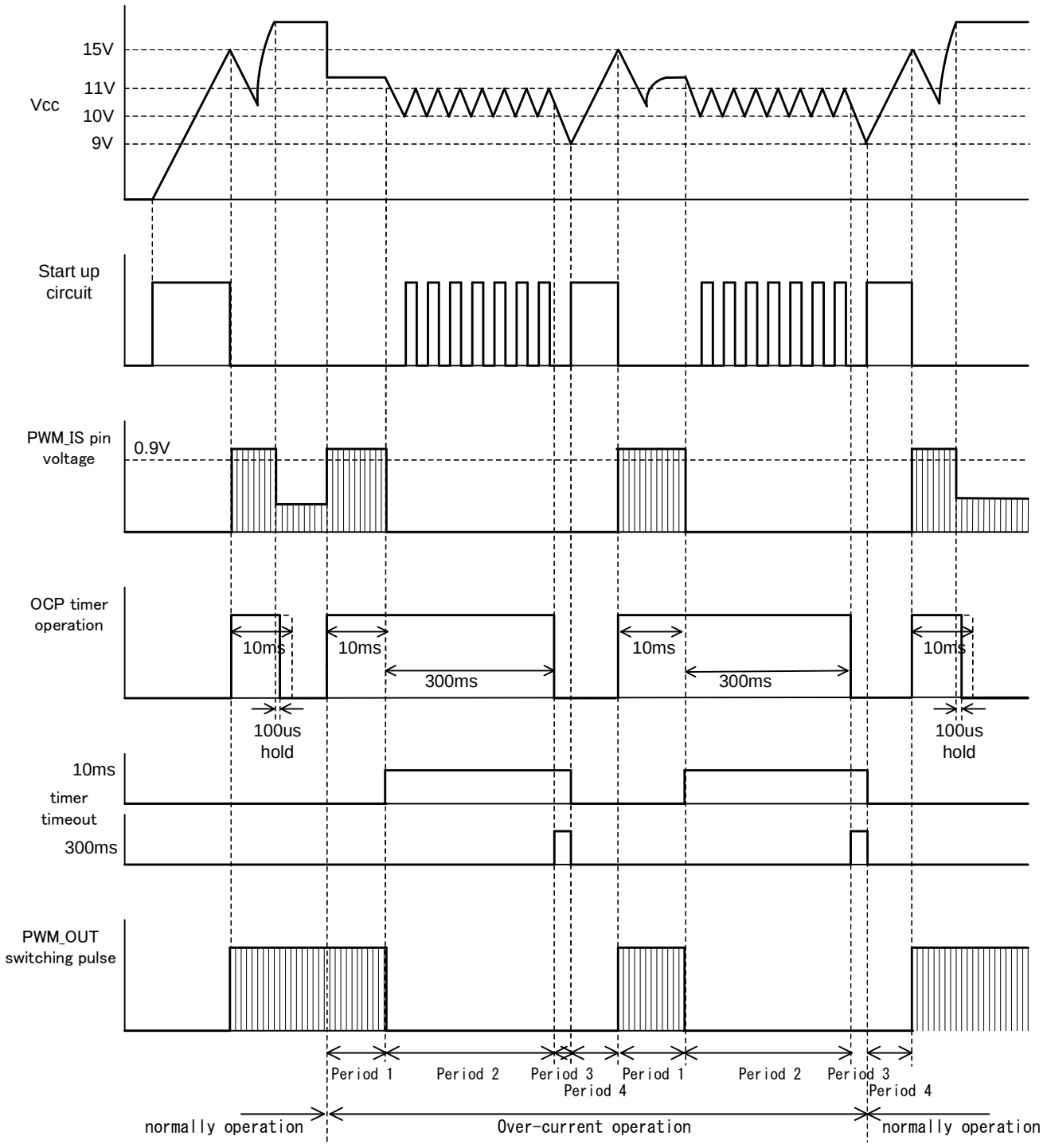

Fig.21 Timing chart from normal current to over-current and return to normal current

9.4 Overvoltage protection

The VCC terminal voltage is monitored, and if it exceeds the threshold level Vccovp26V of VCC terminal overvoltage and this situation continues for the timer-latch time Tov300us or more, operation is shutdown. This state is kept till the input voltage is cut off and till the terminal voltage decreases and reaches the OFF threshold voltage VCCOFF8.5V. Fig. 22 shows the timing chart for overvoltage protection.

Operation can be shutdown forcibly by external signal. Pull up the PWM_IS terminal up to the PWM_IS terminal overcurrent threshold level Visovp1.5V or higher and by keeping this state for the timer-latch delay time Tov300us or more, operation can be shutdown just like in the case of the VCC terminal overvoltage and this state is kept.

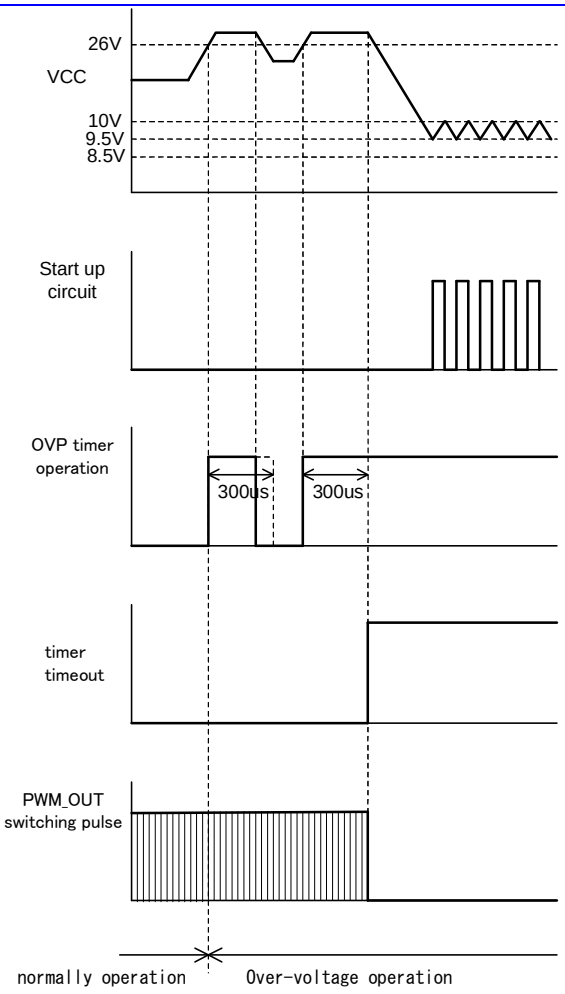

Fig.22 VCC OVP Timing chart from normal operation to over-voltage

10. Overall operation of combined PFC and PWM sections

10.1 Start-up/stop sequence

The following table shows the transition of operation status, and Fig. 23 shows the start-up/stop sequence for it.

State	AC input	STB terminal
(1)	OFF	Low
(2)	ON	Low
(3)	ON	High
(4)	ON	Low
(5)	OFF	Low

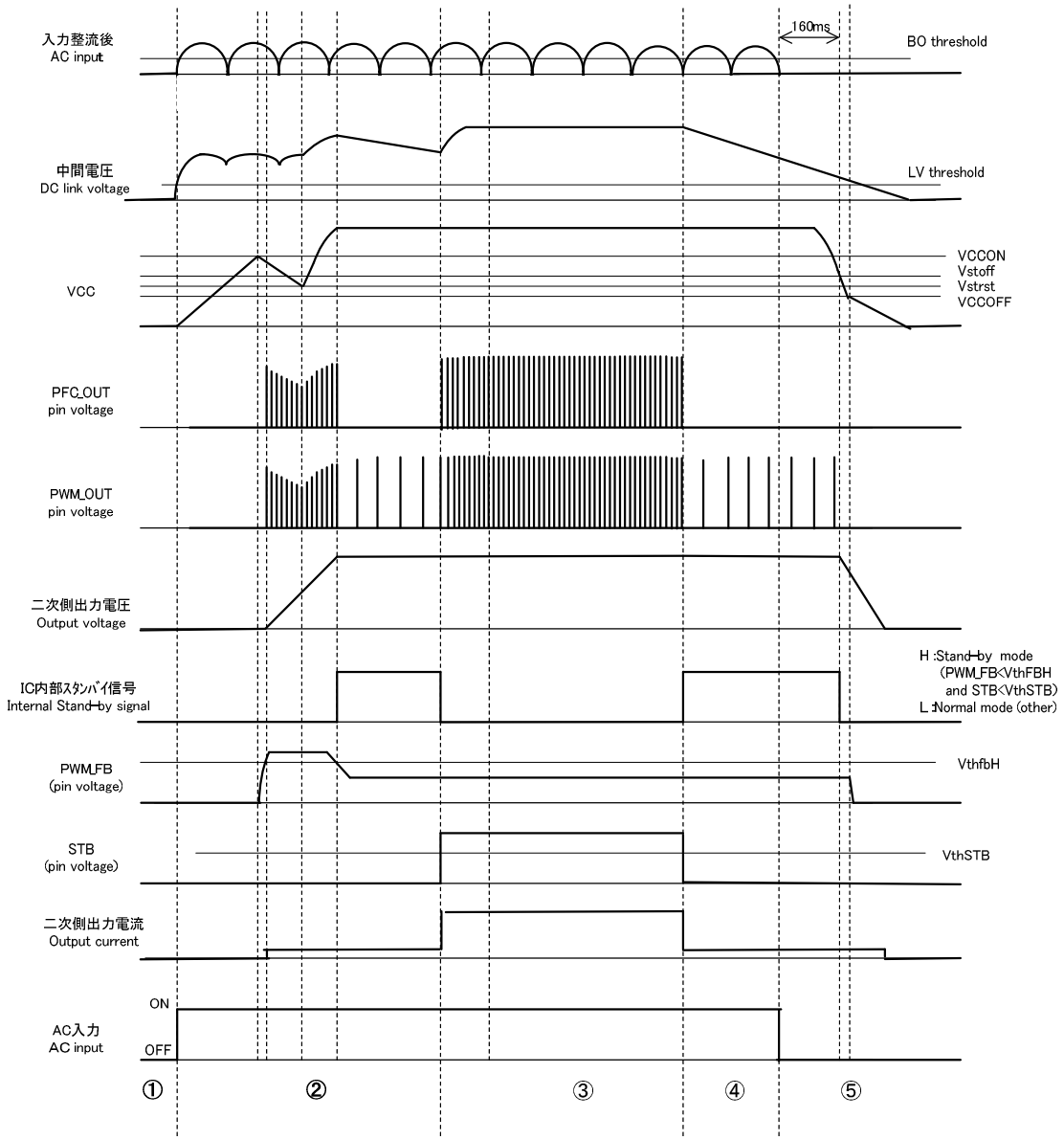

Fig.23 Start-up sequence of standby mode

10.2 Start-up/stop sequence at rated load

The following table shows the transition of operation status, and fig. 24 shows the start-up/stop sequence for it.

State	AC input	STB terminal
(1)	OFF	High
(2)	ON	High
(3)	OFF	High

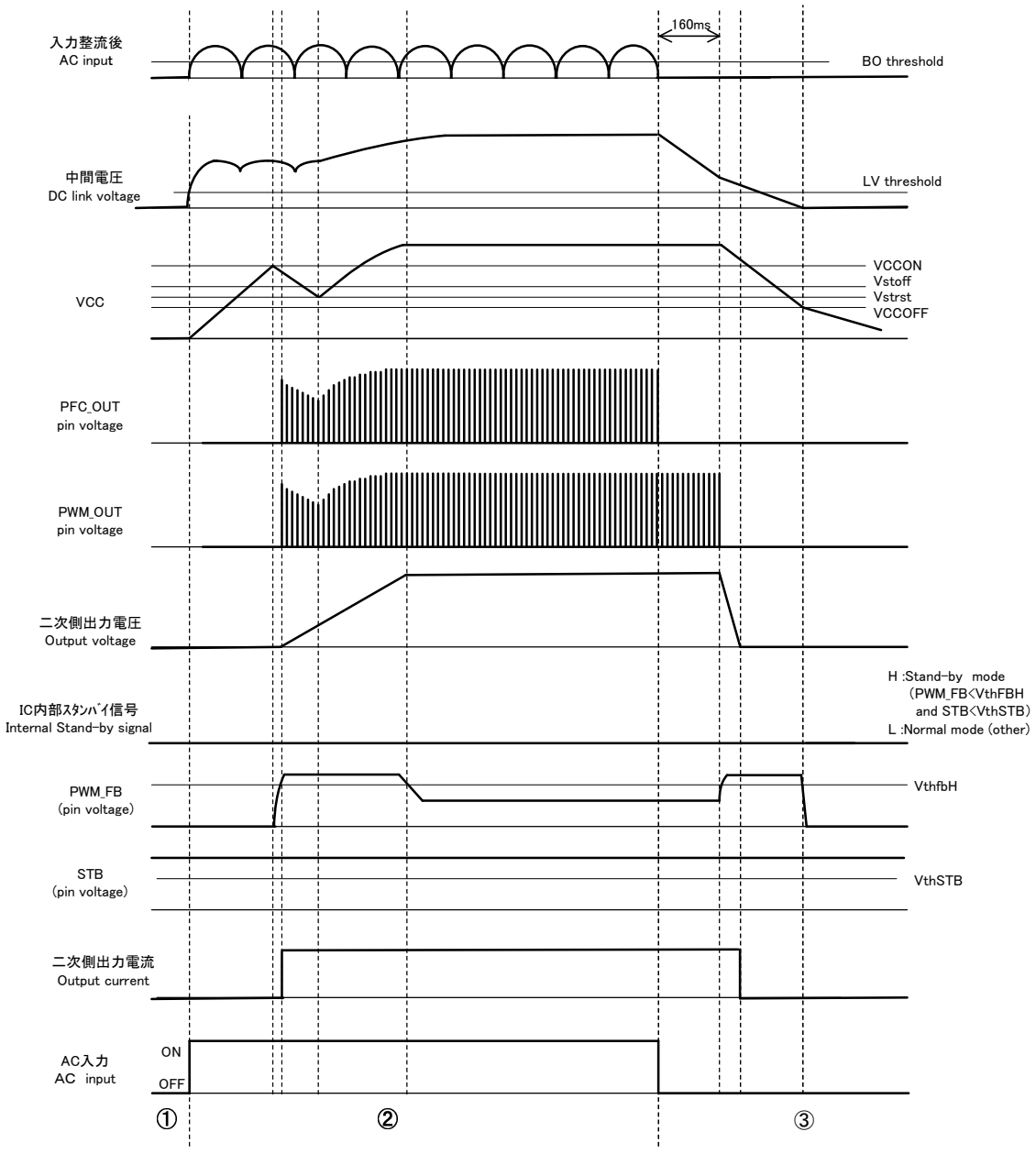

Fig.24 Start-up sequence of normal mode

10.3 Start-up circuit and auxiliary winding voltage

When VCC of this IC is supplied from the transformer's auxiliary winding, the start-up circuit operates and the consumption current increases, and thus careful designing is necessary. Fig. 25 shows an example where sufficient voltage is supplied to VCC. VCC is increased by the start-up circuit to the start-up circuit stop voltage Vstoff0 and starts switching because it exceeds the PWM ON threshold voltage PWM_VCCON. If voltage more than the start-up circuit restart voltage Vstrst is supplied from the auxiliary winding, then the start-up circuit does not operate any more.

Fig. 26 shows an example where the auxiliary winding voltage is not sufficient. If VCC decreases to less than start-up circuit restart voltage Vstrst, the start-up circuit operates and charges the electrolytic capacitor of VCC. When VCC reaches the start-up circuit stop voltage Vstoff, the start-up circuit stops. Although VCC rises and drops repeatedly, switching operation is continued.

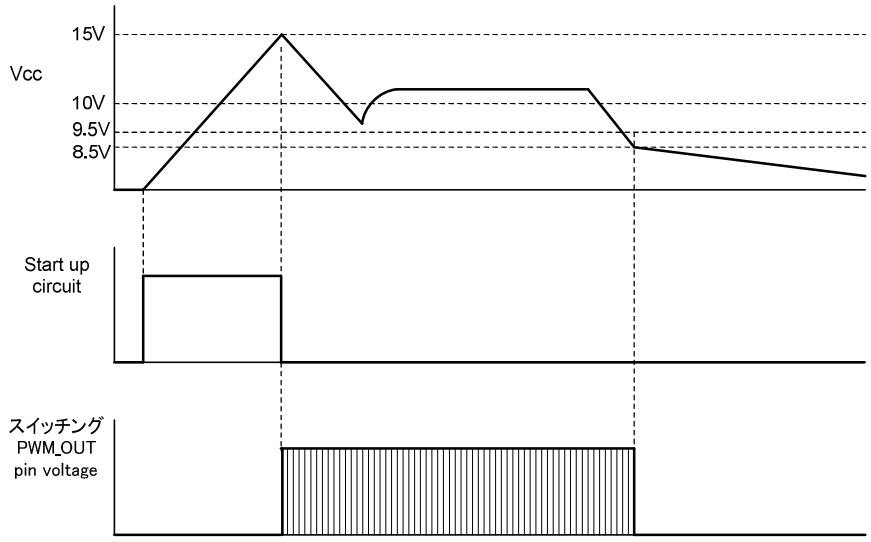

Fig.25 Start/Stop operation (auxiliary winding voltage >9.5V)

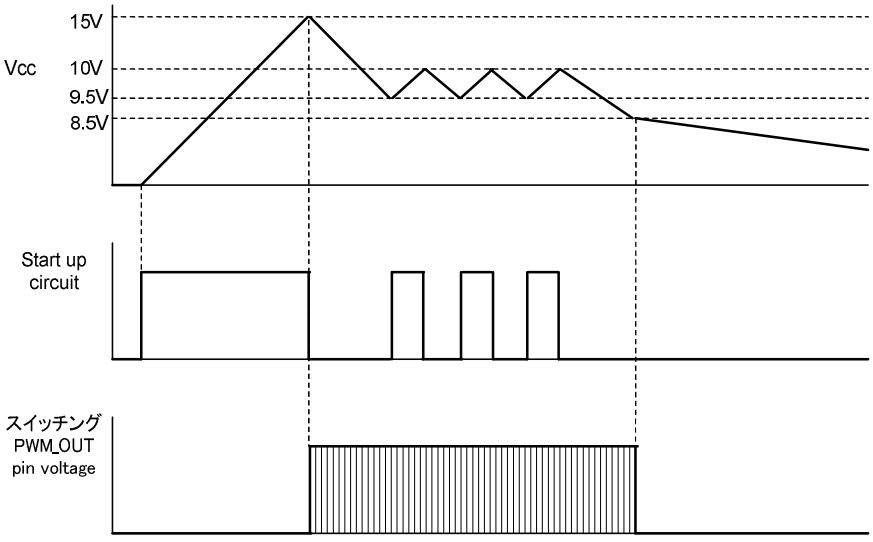

Fig.26 Start/Stop operation (auxiliary winding voltage <9.5V)

11. Advice for designing

11.1 VH terminal (No.1) and VCC terminals (No.3 and 20)

Fig. 27 shows an example of start-up and VCC winding circuit. Since a start-up circuit of max 500V is contained, no external start-up circuit is necessary. When voltage is applied, the start-up current flows from the VH terminal and charges the electrolytic capacitor C2 of VCC. Since charging current depends on the VCC, see the delivery specification for details.

When the VCC voltage reaches the start-up voltage VCCON, the IC starts operation and subsequently power is supplied from the transformer's auxiliary winding P3 to the IC. When the IC starts, the start-up circuit stops operation automatically at the same time.

Fig. 28 shows an example of VCC terminal's waveform during start up. When VCC reaches VCCON, operation starts and consumption current increases. After operation starts, the VCC voltage begins to decrease till power supply from the auxiliary winding starts. If it decreases to Vstrst at this time, the start-up circuit within the IC operates again and helps start-up. Proper selection of start-up resistor R1 and capacitor C2 is necessary so that the VCC voltage does not fall below VCCOFF. Insert R2: 2.2Ω or more shown in Fig. 27 in the VCC winding circuit. This is because, at start-up, short operation occurs since charge of C2 and C4 is empty, and the VW voltage described later cannot be generated easily and normal operation cannot be performed. Since the IC is a C-MOS type, connect C1 and C3 by-pass capacitors of 0.1μF or over very near the terminals between the VCC and GND terminals.

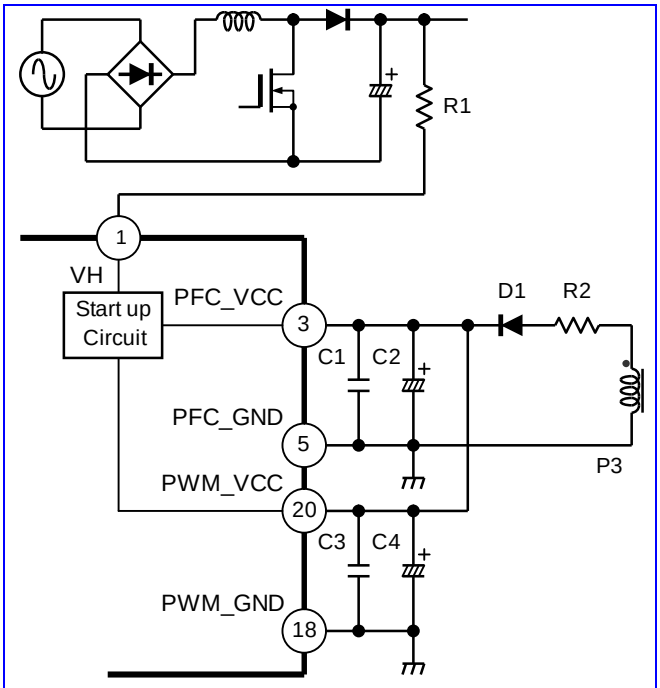

Fig.27 Start-up and VCC Winding Circuit

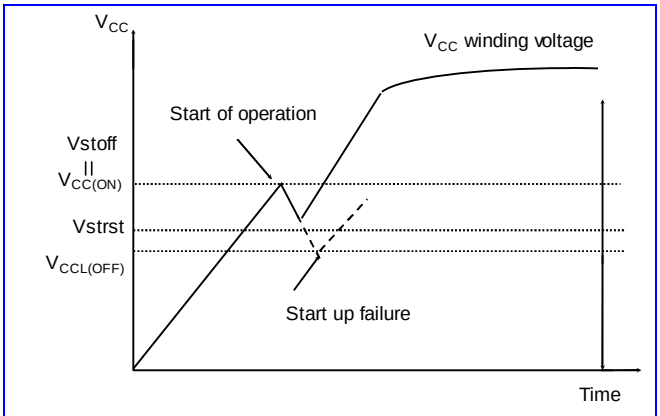

Fig.28 Example Waveform of VCC Terminal at Start-up

11.2 PFC_OUT (No.4) and PWM_OUT terminals (No.19)

They are connected to the gate terminals through resistors. While MOSFET is turned on, the OUT terminal voltage is in a high level and almost the VCC voltage is output. While MOSFET is turned off, the OUT terminal voltage becomes a low level and almost 0V is output.

An example of connection is shown in Fig. 29. By separating the gate resistors for turn-on and turn-off, switching speed can be set separately.

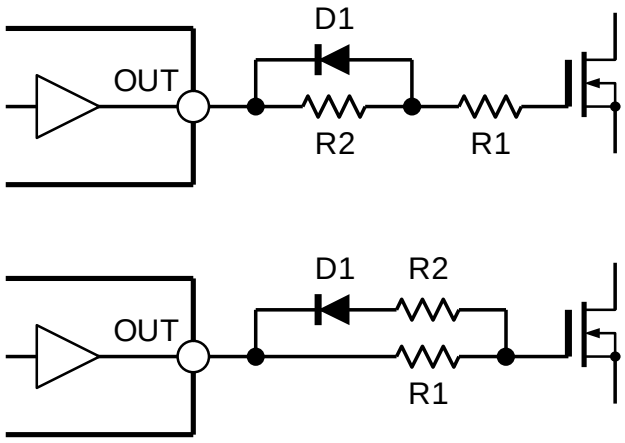

Fig.29 MOSFET Gate drive circuit

Connect the PWM_OUT terminal (No.19) to MOSFET (Q1) in the lower part of the current resonance circuit. The gate drive of the upper-side MOSFET (Q2) uses the transformer's auxiliary winding voltage.

11.3 PFC_ZCD terminal (No.6)

Auxiliary winding voltage of L1 is input to the PFC_ZCD terminal to detect the timing for turn-on of MOSFET. Since the current that is flowed to the ZCD terminal is used in the IC rating, usually the resistor R1 for current limiting is inserted between the ZCD terminal and the auxiliary winding. Voltage of auxiliary winding is always changing against each instantaneous value of AC input as shown in Fig. 31. Based on this operation, each condition is obtained.

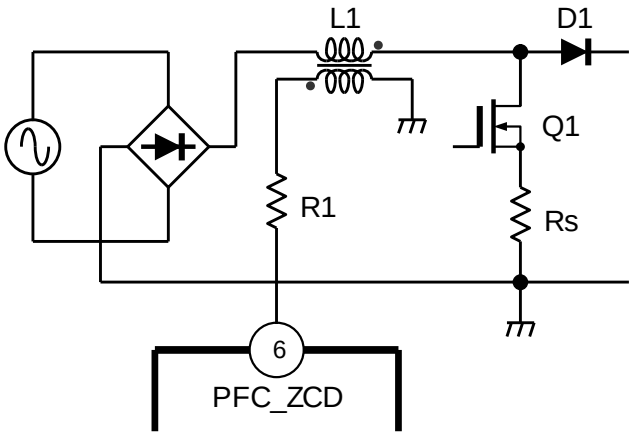

Fig.30 PFC_ZCD terminal circuit

The threshold voltage of the ZCD comparator is 1.65V (max.) at startup. The following conditional expression shall be satisfied because, even when voltage of the auxiliary winding becomes the smallest, it should exceed the threshold voltage.

$$Ns / Np > \frac{1.65}{(Vo - \sqrt{2} \times Vac(\max))}$$

In order to operate normally, however, it is necessary to limit the current Izcd, which is flowed to the clamp circuit of the ZCD terminal, to 3mA or lower. The following relational expressions shall be satisfied for this reason.

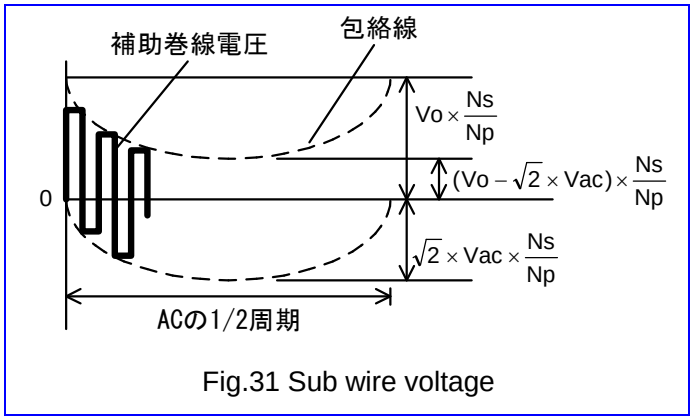

Fig.31 Sub wire voltage

$$\text{During On} > \frac{1.0 + \sqrt{2} \times \text{Vac(max)} \times \frac{\text{Ns}}{\text{Np}}}{3 \times 10^{-3}}$$

$$\text{During Off} : \text{R1} > \frac{\text{Vo} \times \frac{\text{Ns}}{\text{Np}} - 7.0}{3 \times 10^{-3}}$$

If resistance is big and current that is flowed to the clamp circuit is too small, stable operation cannot be made. Therefore R1 shall be smaller than 47kΩ.

11.4 PFC_IS terminal (No.7)

Largest threshold voltage of the PFC_IS terminal should be 0.85V min. The current detecting resistor Rs is set to flow the necessary current for this min value of Vthis. The max value $I_{LP(max)}$ of the inductor's peak current can be almost expressed in the following formula:

$$I_{LP(max)} = \frac{2 \times \sqrt{2} \times Po}{\eta \times Vac_{(min)}}$$

Accordingly the value of Rs can be obtained as follows:

$$Rs = \frac{V_{thIS}}{I_{LP(max)}} = \frac{1.3}{I_{LP(max)}}$$

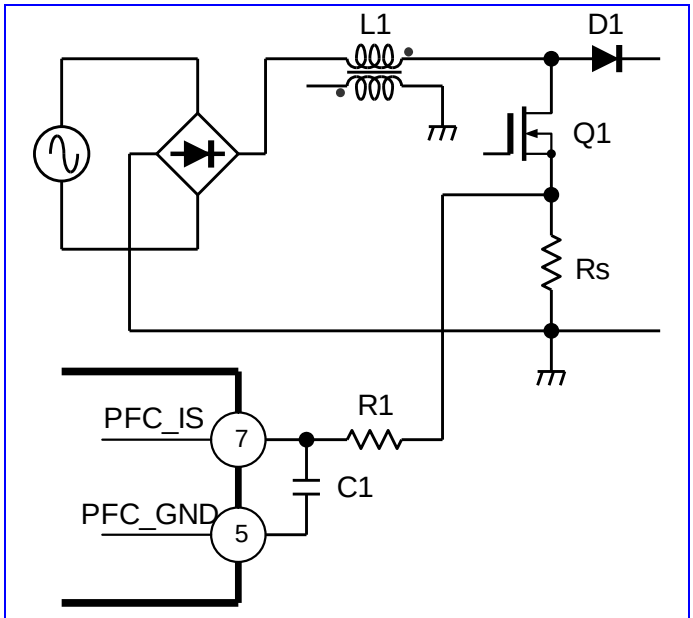

Fig.32 PFC_IS terminal circuit

If the PFC_MUL terminal's peak voltage is 1.4V or lower, however, Rs should be smaller than the above set value.

When MOSFET is turned on, the gate drive current of MOSFET and the surge-like current caused by discharge of circuit's parasitic capacitance flows to the current detecting resistor Rs. This IC controls the peak value of the current flowing to MOSFET, and if this surge-like current is

large, the input current waveform may become unstable due to a malfunction. In addition in some cases, whisker-shaped pulses may be mixed in the turn-on section of the IC's OUT pulse, depending on size and timing of the surge-like current. Therefore usually the CR filter is connected. The cutoff frequency of this filter should be set sufficiently higher than the switching frequency so as not to affect the usual operation. The cutoff frequency is set to 1 to 2MHz here.

$$\frac{1}{2\times\pi\times C1\times R1}\approx 1\text{ to }2\,[\mathrm{MHz}]$$

11.5 PFC_MUL terminal (No.8)

The peak voltage of the PFC_MUL terminal depends on change of the AC input voltage. If the MUL terminal voltage is set to 1.4V or lower, current is limited by the multiplier's output and cannot flow up to the IS max threshold. Thus usually the MUL terminal peak voltage is set to about 1.4V to 5.0V.

$$V_{MUL-P(min)} = \sqrt{2}\times Vac(min)\times\frac{R2}{R1+R2} > \text{About } 1.4\,[V]$$

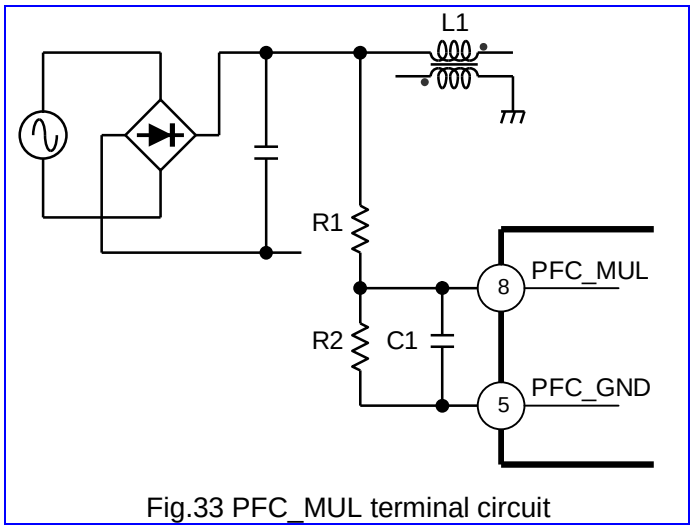

Fig.33 PFC_MUL terminal circuit

In the actual circuit, voltage after rectification contains a lot of noises caused by switching. Usually the capacitor C1 is connected between the PFC_MUL and PFC_GND terminals to eliminate the influence of noises. IF the value of C1 is small, effect of the filter becomes weak, and if it is too large, the waveform of the AC input voltage which is input into the PFC_MUL terminal is distorted. In a desk study, set the cutoff frequency decided by C1, R1 and R2 to about 1 to 2kHz.

$$\frac{1}{2\times\pi\times C1\times(R1//R2)}\fallingdotseq 1\text{to }2\,[\mathrm{kHz}]$$

$R1 // R2$ is the combined resistance of $R1$ and $R2$ connected in parallel.

11.6 PFC_COMP terminal (No.9) and PFC_FB terminal (No.10)

The output voltage Vo of PFC is controlled so that the voltage, which is input into the FB terminal after resistance voltage division, matches the interior reference value. The relation between Vo and the voltage-dividing resistor is as follows.

$$Vo = Vfb\_pfc \times \frac{R1 + R2 // 1M}{R2 // 1M}$$

$R2 // 1M$ is the combined resistance of $R2$ and $1M$ connected in parallel.

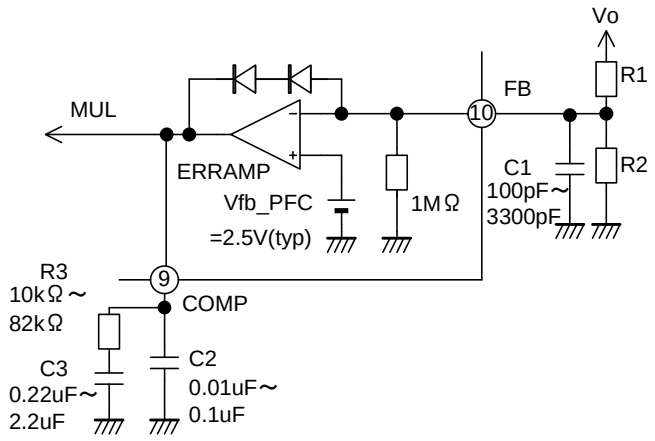

Fig.34 PFC_COMP, PFC_FB terminal circuit

Output of PFC contains the ripple voltage of frequency double the AC input voltage. If this ripple appears in the input/output of the error amplifier, PFC does not operate stably. Therefore a capacitor or resistor is connected between the FB-GND terminals and between the COMP-GND terminals respectively for phase correction. However, using the constants shown in Fig. 34, adjustment is necessary for phase correction of the error amplifier's output because the power factor, stable operation and responsiveness are in the trade-off relation.

Improvement of power factor: R3= small resistance value, C2 and C3=large capacity

Improvement of transient responsiveness and stable operation: R3= large resistance value, C2 and C3=small capacity

11.7 VREF terminal (No.11)

5V is produced from the VCC voltage by the regulator and output to the exterior. Since the IC is C-MOS, connect the capacitor C1 very near the VREF-GND terminals as shown in Fig. 35. Preferably the capacity of C1 should be 1μF or more.

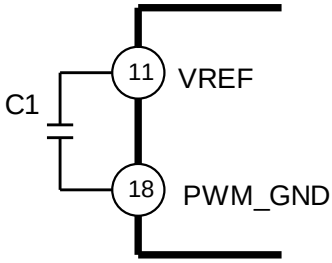

Fig.35 VREF Terminal

11.8 STB terminal (No.12)

The STB terminal is the input terminal for the signal switching the standby/normal operation. If the STB terminal is made to be the threshold voltage Vstbon1.0V or lower, transfer to the standby mode is performed. To release the standby mode to transfer to the normal operation mode, have it at the threshold voltage Vstboff2.5V or more. Example of circuit is shown in the figure.

11.9 PWM_CB terminal (No.13)

A capacitor is connected between the PWM_CB-GND terminals to set the oscillating frequency of the CB terminal. Continuous saw-toothed waveform is created by charging and discharging the capacitor.

11.10 PWM_CS terminal (No.14)

A capacitor is connected between the PWM_CS-GND terminals to set the slope (dv/dt) of the CS terminal voltage. A triangular waveform is created by charging and discharging the capacitor. This slope of CS terminal voltage is used for the soft start/soft end function during the standby operation.

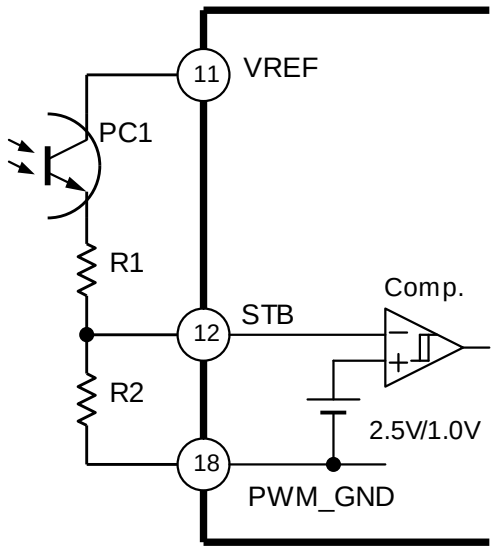

Fig. 36 STB Terminal

Widen the pulse width gradually when the slope is ascending and narrow the width gradually when it is descending to reduce the abnormal sound from the transformer.

11.11 PWM_FB terminal (No.15)

The PWM_FB terminal is the input terminal of the feedback signal for control of the secondary-side constant voltage. Fig. 37 shows an example circuit around the PWM_FB terminal. If the transient response is not stable, connect C1 and R1 to reduce the feedback gain and adjust the constant.

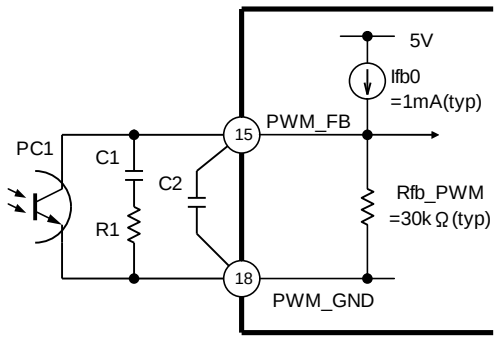

Fig.37 PWM_FB Terminal

In addition, connect C2 (about 0.1u) very near the PWM_FB-PWM_GND terminals to prevent a malfunction caused by noises. Keep the wiring distance from PC1 as short as possible so that there is no influence from other current.

11.12 PWM_IS terminal (No.16)

The Q1 drain current is converted into voltage by the detecting resistor Rs and input into the PWM_IS terminal. Detection is conducted in the plus polarity against DND. Rs is obtained by the following formula (in the case of Id1=5A):

$$Rs = \frac{Voc}{Id1} = \frac{0.9V(\max.)}{5} = 0.18\Omega$$

Since the current flowing in Q1 when the input voltage is low becomes large, set Rs by using Id1 for the time when the input voltage is the smallest value (standard min).

Insert the shot key diode Ds very near the PWM_GND and Q1 source terminals. This is performed not to apply minus voltage to the IC and to prevent an accidental turning-on of Q1 caused by wiring inductance in the IS terminal – Rs –GND terminal. It is advised to use ERA82-004 (40V/0.6A) produced by us for Ds.

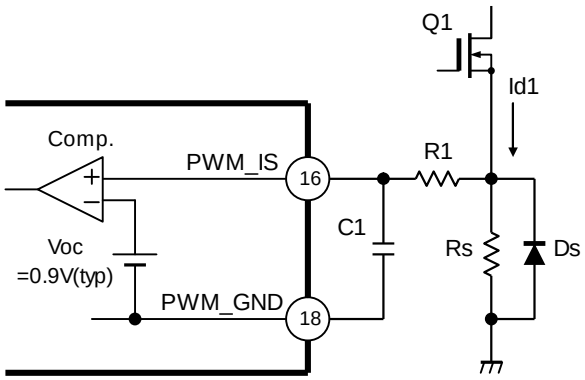

Fig. 38 PWM_IS Terminal

However, checking is necessary because the diode duty changes depending on pattern layout and test conditions. If noises are applied to the IS terminal, insert filters of R1 and C2. Filter's corner frequency fs can be obtained by the following formula. Select fs to be 100kHz to 1MHz.

$$fs = \frac{1}{2\pi C2R1}$$

11.13 PWM_VW terminal (No.17)

Fig. 39 shows an example circuit around the VW terminal. The VW terminal detects the polarity of the main winding P1 by using the transformer's auxiliary winding P3.

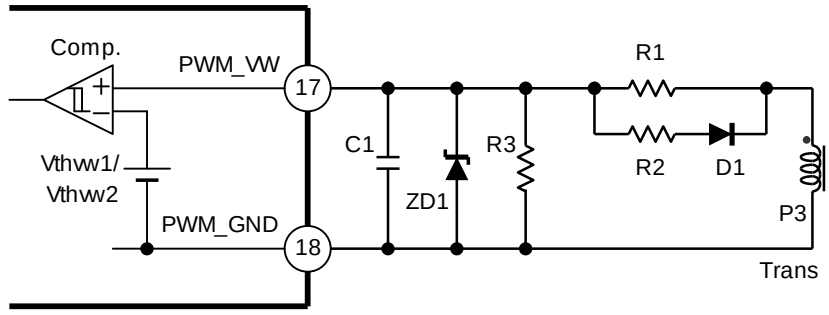

Fig. 39 PWM_VW Terminal

Q2 is turned off, the signal of VP3's polarity changing from negative to positive is received and Q1 is turned on after the delay time Tdvw set within the IC passes. Furthermore when VP3 becomes negative from positive, Q1 is forcibly turned off.

The VW signal is input into the comparator, Q1 ON threshold value Vthvw2 = 1.6V (typ.) and Q1 OFF threshold value Vthvw1 = 0.6V (typ.). The zener diode ZD1 of 4.5V or less is connected between VW-GND terminals to protect the IC because the comparator operates at the reference voltage VREF. C1 is connected to prevent simultaneous turn-on of C1 and C2 and to delay turn-on of Q1. The VW terminal voltage should sufficiently exceed Vthvw to perform continuous oscillation within the power supply specifications. In addition, have the value of R2 as small as possible because Q1 is turned off forcibly in the timing when the VW terminal voltage falls below the Vthvw1.

It is advised to use the following values for the respective constants, but checking is necessary by conducting a test.

R1: 3.3 to 10kΩ、R2: 1kΩ to 5.6kΩ、R3: 100kΩ、C1: 220 to 820pF、ZD1: 3.9V

11.14 MOSFET (Q2) drive circuit

Transformer's auxiliary winding voltage is used to drive the high-side MOSFET (Q2). An example of Q2 drive circuit is shown in Fig. 40 and the method of setting the circuit constants is shown below.

R1 and R3 are the resistors to decide the turn-off speed of Q2. About 47Ω is recommended for R1 and about 39Ω for R3.

R1 and R2 are the resistors to decide the turn-on speed of Q2. The value satisfying the following two conditions should be set for R2.

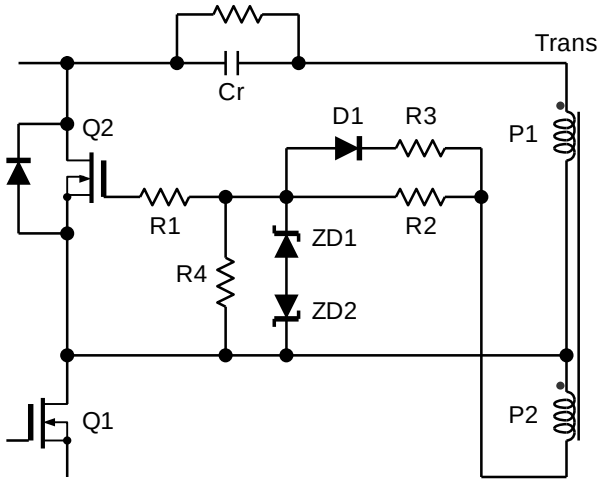

Fig.40 Q2 Drive Circuit

Condition (1)

Setting should be made so that Q2 turns on while current is flowing in the body diode of Q2 after Q1 turns off.

Condition (2)

Setting should be made so that an arm short circuit does not occur when Q2 is turned on in startup. (Checking should be made after completely discharging the electrolytic capacitor of the VCC winding.)

R4 is inserted so that the Q2 gate voltage is not lifted at dv/dt of the drain voltage of Q2. About 22kΩ is recommended. ZD1 and ZD2 are connected to keep the voltage below the absolute maximum rating for the voltage between Q2 gate and source.

Check that the Q2 gate voltage sufficiently exceeds the gate threshold voltage Vgs(th) while starting operation or when DC input voltage fluctuates. If the Q2 drive voltage is not generated sufficiently, oscillating operation cannot be continued.

11.15 Design of PFC inductor

Decide power supply specifications for the following before starting design.

Range of input voltage (Vms): Vac (min) to Vac (max)

Output voltage (V): Vo ($> \sqrt{2} \times \mathrm{Vac(max)}$)

Max. output power (W): Po

The converter for power-factor improvement uses the voltage-increasing system for the circuit system, and thus the output voltage Vo should be set higher than the peak value ($= \sqrt{2} \times \mathrm{Vac(max)}$) of the input voltage. Since the critical mode PFC uses self-oscillation, the switching frequency is decided by the input/output conditions and inductor value. (See the complement.)

The inductance Lp is decided from the input/output conditions and the minimum operating frequency. When the PFC efficiency is η and the min operating frequency is fsw(min.), it can be obtained by the following formula:

$$Lp = \frac{Vac_{(\min)}{}^{2} \times (Vo - \sqrt{2} \times Vac_{(\min)}) \times \eta}{2 \times fsw(\min.) \times Po \times Vo}$$

Use the guideline of 20kHz to 100KHz to decide fsw(min.). Assume efficiency η to be about 90% in designing.

<Complement: Inductance and switching frequency>

The On and Off states in the input/output conditions and the respective cycles can be expressed in the following formulas theoretically:

$$\mathrm{Ton} = \frac{2 \times \mathrm{Lp} \times \mathrm{Po}}{\mathrm{Vac}^2 \times \eta}$$

$$\mathrm{Toff} = \frac{2 \times \mathrm{Lp} \times \mathrm{Po}}{\mathrm{Vac}^2 \times \eta \times \left(\frac{\mathrm{Vo}}{\sqrt{2} \times \mathrm{Vac} \times |\sin \omega t|} - 1 \right)}$$

$$\text{However } \omega = 2 \times \pi \times \mathrm{fac}$$

$$\mathrm{fac}: \text{Frequency}[\mathrm{Hz}] \text{ of AC input voltage}$$

Therefore if the input/output conditions are constant, theoretically Ton becomes constant. On the other hand, Toff changes against each momentary value of AC input and becomes maximum at ωt=90° and minimum at ωt=0°. From the above relation, switching frequency becomes as follows:

$$fsw = \frac{Vac^2 \times \left(Vo - \sqrt{2} \times Vac \times |\sin \omega t|\right) \times \eta}{2 \times Lp \times Po \times Vo}$$

As shown above, it constantly changes against each momentary value of AC input.

11.16 Design of current-resonance transformer

Fig. 23 shows configuration of the transformer. Power is supplied form the input voltage Ed to the current-resonance transformer during the Q1 ON state Ton(Q1) in one cycle T and a part of it is converted to the secondary-side output. At the same time, energy is stored in the resonant capacitor Cr.

Subsequently the energy stored in Cr is discharged to the secondary side during the Q2 ON stage. On-Duty becomes 50% in the max output.

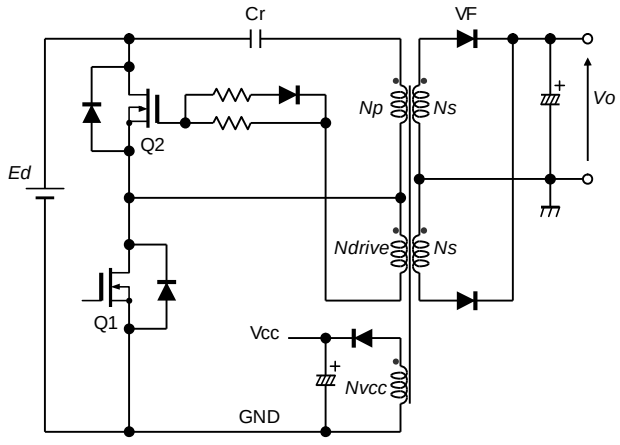

Fig.41 Transformer Configuration

(1) Definition of each constant/variable

Input DC voltage: Ed(V), output voltage: Vo(V), voltage drop of output diode: VF(V)
Output current: lo(A), output voltage: Po(W), conversion efficiency of converter: η, switching frequency: f(Hz), primary-side inductance Lp (=Lm+Lr), vacuum transmittance of core: μo(H/m), gap length: lg(mm), effective cross section of core: Ae(mm2), effective magnetic path length of core: lc(mm), magnetic flux density: Bc(T), amplitude permeability: μc

(2) Conversion efficiency η

η is assumed to be 0.93 (η = 0.93), and the targeted output power Po is calculated.

$$Po = \frac{(Vo + VF)Io}{\eta} \quad \cdots\cdots(1)$$

(3) Transformer applied voltage Vp

1/2 of Ed is applied to the primary-side winding of transformer.

$$Vp = \frac{Ed}{2} \quad \cdots\cdots(2)$$

Substitute the minimum value Ed(min) into Ed.

(4) Primary-side inductance Lp

$$Lp = \frac{\mu o\left(\frac{VpTon}{Bc}\right)^2}{\left(\frac{lc}{\mu c} + lg\right)Ae} \quad \cdots\cdots(3)$$

Ton is the value decided by frequency T and Duty=0.5.

(5) Number of primary-side winding turns Np

$$Np = \sqrt{\frac{Lp\left(\frac{lc}{\mu c} + lg\right)}{\mu oAe}} \quad \cdots\cdots(4)$$

(6) Magnetic flux density

$$Bc = \frac{\mu oNpI_{lm}}{\frac{lc}{\mu c} + lg} \quad \cdots\cdots(5)$$

llm stands for exciting current, and $I_{lm} = \frac{VpTon}{Lp}$

It is necessary to see the specifications of the used core material, but usually it is held to 0.25T or less.

(7) Number of secondary-side winding turns Ns

$$Ns = \frac{Vo + VF}{Vp} Np \quad \cdots\cdots(6)$$

Number of turns Ns obtained from calculation is rounded to an integer.

(8) Recalculation of Np and Lp

$$Np = Ns \frac{Vp}{Vo + VF} \quad \cdots\cdots(7)$$

$$\mathrm{Lp} = \frac{\mu o \mathrm{AeNp}^2}{\frac{\mathrm{lc}}{\mu c} + \mathrm{lg}} \quad \cdots\cdots(8)$$

Round the number of turn Np obtained from calculation to an integer. Adjust the gap length to keep Lp within the range of 1.6 to 1.8mH. This is because the transformer's exciting energy should be bigger than the energy for charging and discharging the output capacity of Q1 and Q2 to perform zero-volt turn on/off of Q1 and Q2.

(9) Leakage inductance Lr

$$Lr \cong \left(\frac{Np}{Np'} \right)^2 Lr' \quad \cdots\cdots(9)$$

Leakage inductance Lr caused by binding degree of winding is decided mainly by structure such as bobbin shape and winding method and thus it is difficult to calculate it in advance. In this section, it is obtained by using Lr' when measurement data of the same structure is Np'.

(10) Resonance frequency fr and max. output power Po

$$fr = \frac{1}{2\pi\sqrt{LrCr}} \quad \cdots\cdots(10)$$

$$Po \cong CrEd^2 fr = \frac{Ed^2}{2\pi}\sqrt{\frac{Cr}{Lr}} \quad \cdots\cdots(11)$$

Although it depends on application of power supply, the recommended value of resonance frequency fr is 25 to 90kHz.

(11) Gap length lg

$$\mathrm{lg} = \frac{\mu o \mathrm{AeNp}^2}{\mathrm{Lm}} - \frac{\mathrm{lc}}{\mu c} \quad \cdots\cdots(12)$$

The above formula is derived from the formula (8).

(12) Number of turns of Q2 drive winding Ndrive

$$Ndrive = \frac{Vgs}{Ed(\max)} Np \quad \cdots\cdots(13)$$

Vgs is the voltage applied between Q2 gate and source, and it should not exceed the VGS absolute max rating of 30V at the max input voltage Ed(max).

(13) Number of turns of control power supply voltage

$$Nvcc = \frac{Vcc}{Ed(\min)} Np \quad \cdots\cdots(14)$$

Vcc is the min operating voltage for the control IC built-in with M-Power, and design should be made so that the Vcc terminal voltage does not fall below VccL(off). For Ed(min), consider the min value of the AC input voltage.

Example design of transformer

Description is made about an example of designing the transformer in the conditions shown in the following table.

Item	Symbol	Set value
Input DC voltage	*Ed*	350~390V
Output voltage	*Vo*	24V
Output current	*Io*	10A
Output power	*Po*	240W
Type of core		EPC53
Effective cross section	*Ae*	194.9 mm^2
Effective magnetic path length	*Le*	132.6mm
Leakage inductance	*Lr*	95uH @Np=26T

The design results are shown in the following table.

Item	Symbol	Set value
Number of turns on primary side	*Np*	42T
Number of turns on secondary side	*Ns*	6T
Number of turns of Q2 drive winding	*Ndrive*	3T
Number of turns of Vcc winding	*Nvcc*	5T
Primary-side inductance	*Lp*	1.8mH
Leakage inductance	*Lr*	248uH
Gap length	*lg*	196um
Resonance frequency	*fr*	42.7kHz
Resonant capacitor	*Cr*	56nF

Connecting diagram and sectional view of the transformer are shown below. The block structure is recommended for the bobbin to secure the sufficient leakage inductance. Decide the wire cross section so that the current density is about 4A/mm^2 to restrict temperature rise of the transformer. The higher the frequency of switching is, the higher the loss caused by conductor skin effect is, and thus it is advised to use a Litz wire.

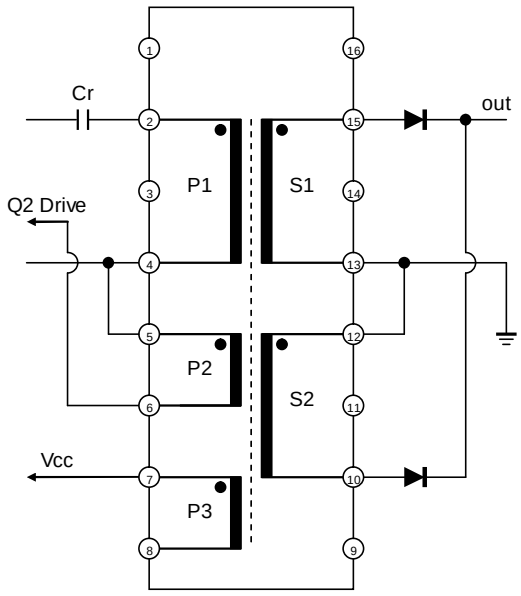

Fig.42 Transformer wiring connection

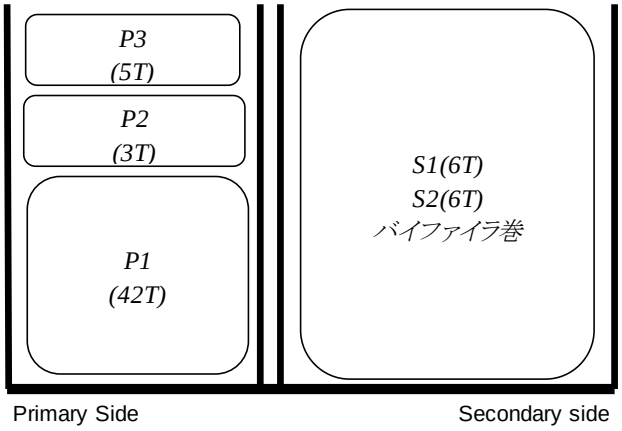

Fig.43 Transformer cross section

11.17 Design of pattern layout

1. Separate the minute current paths of control system such as the main current path, gate current path and feedback so that there is no mutual interference among them.
2. Wire PFC_GND and PWM_GND branched on the minus side of the electrolytic capacitor C1. This is necessary to prevent a malfunction caused by interference of PFC operation and current resonance operation.
3. Connect the capacitor C2 very near a place between the VREF and PWM_GND terminals.
4. Connect the capacitor C3 very near a place between the PFC_VCC and PFC_GND terminals.
5. Connect the capacitor C4 very near a place between the PWM_VCC and PWM_GND terminals.
6. Wiring among the PWM_FB and PWM_GND terminals and PC1 should be as short as possible and separated from other patterns because minute electric current of 1mA or lower flows in them. This wiring should also be located as far away as possible from the main current path.
7. Do not set any electronic part immediately below the inductor or transformer and do not draw any control-system pattern right below it.

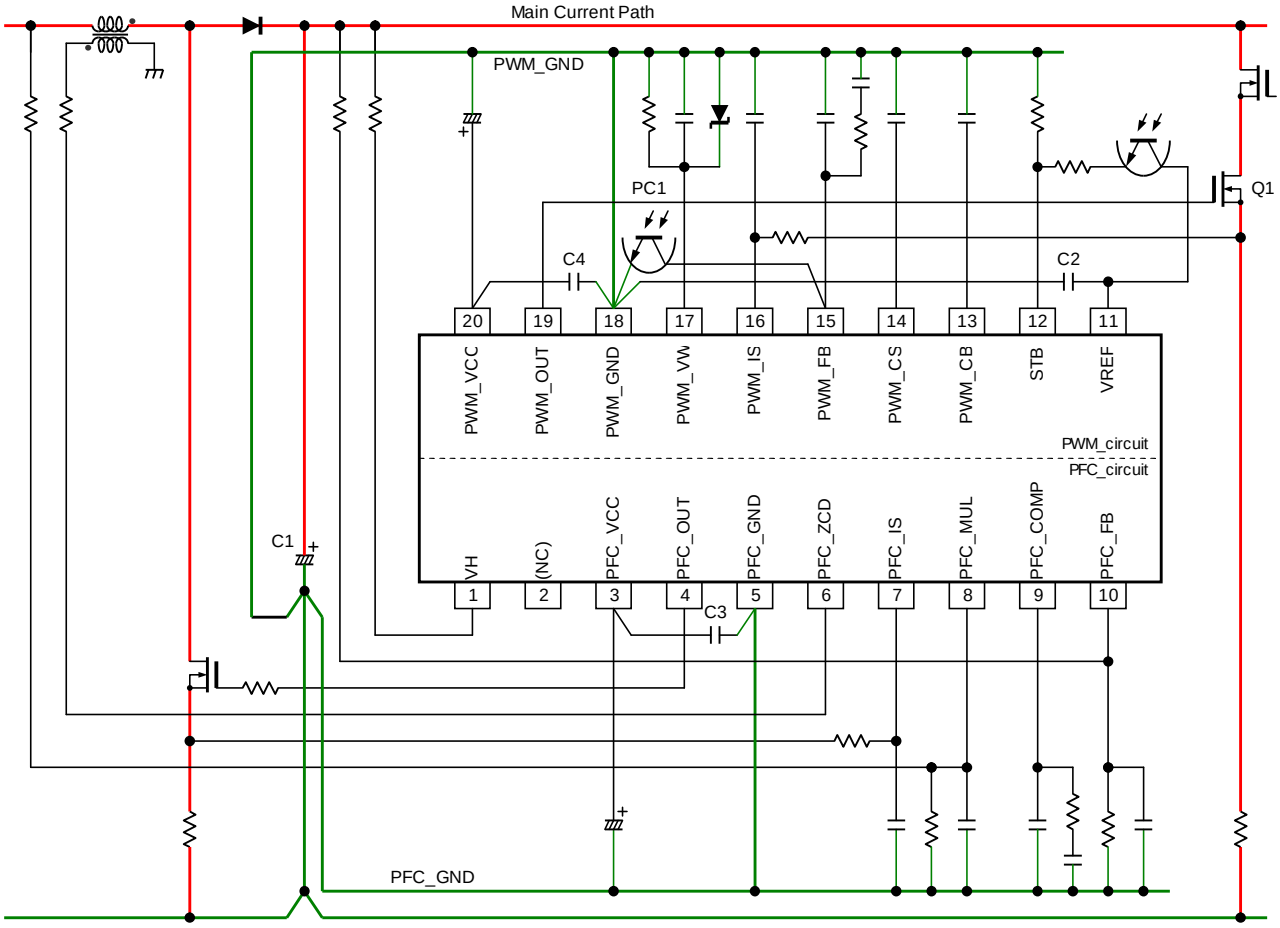

Fig.44 Pattern layout Design

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