Fuji Switching Power Supply Control IC

FA5596/97

Application Note

NOV.-2009
Fuji Electric Systems Co., Ltd.

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Caution)

・The contents of this note subject to change without notice due to improvement.

・The application examples or the parts constants in this note are shown to help your design.
Variation of parts and service condition are not fully taken into account.
Before use, a design with due consideration for these variations and conditions shall be conducted.

1. Overview

FA5596/97 is a current mode type switching power supply control IC possible to drive a power MOSFET directly. Despite of a small package with 8 pins, it has a lot of functions and it is best suited for power saving at the light load and decreasing external parts. Moreover it enables to realize a reduced space and a high cost-performance power supply.

2. Features

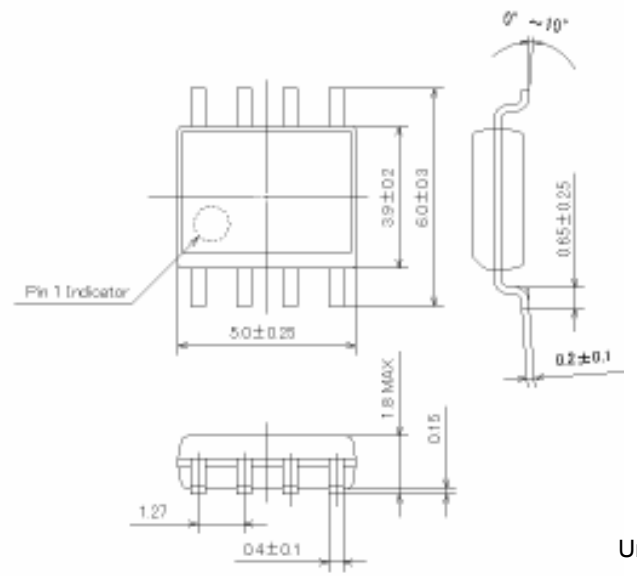
- Excellent Power Saving by lowering the oscillation frequency depending on the load at light load.
- Low power consumption by a built-in startup circuit.
- Current Minus detection. Power Saving of the revision of the input voltage of OLP.
- Overload protection function with a few number of external components. Auto Recovery type or Timer Latch type.
- Two-stages Over Load Protection suitable for Motor Driving.（FA5596/97）
- Brown-In/Out Function without additional external components.
- Latch pin for an external signal: Over Temperature Protection, Over Voltage Protection etc.
- External MOSFET driving suitable for Power Supply up to 200W: -1.0A(sink),/+0.5A(source)
- VCC Under-Voltage Lock-Out function (UVLO). (Vcc=18V/9V)

Function list

Part Number	Switching frequency	OLP Type	IS pin VthIS	FB pin VthFB	OLP Delay time	OLP restart time
FA5596	65kHz	Auto Recovery	VthIS=-0.5V	VthFB=2.8V	70ms	1530ms
FA5597	65kHz	Latch	VthIS=-0.5V	VthFB=2.8V	70ms	—

3. Outline drawing

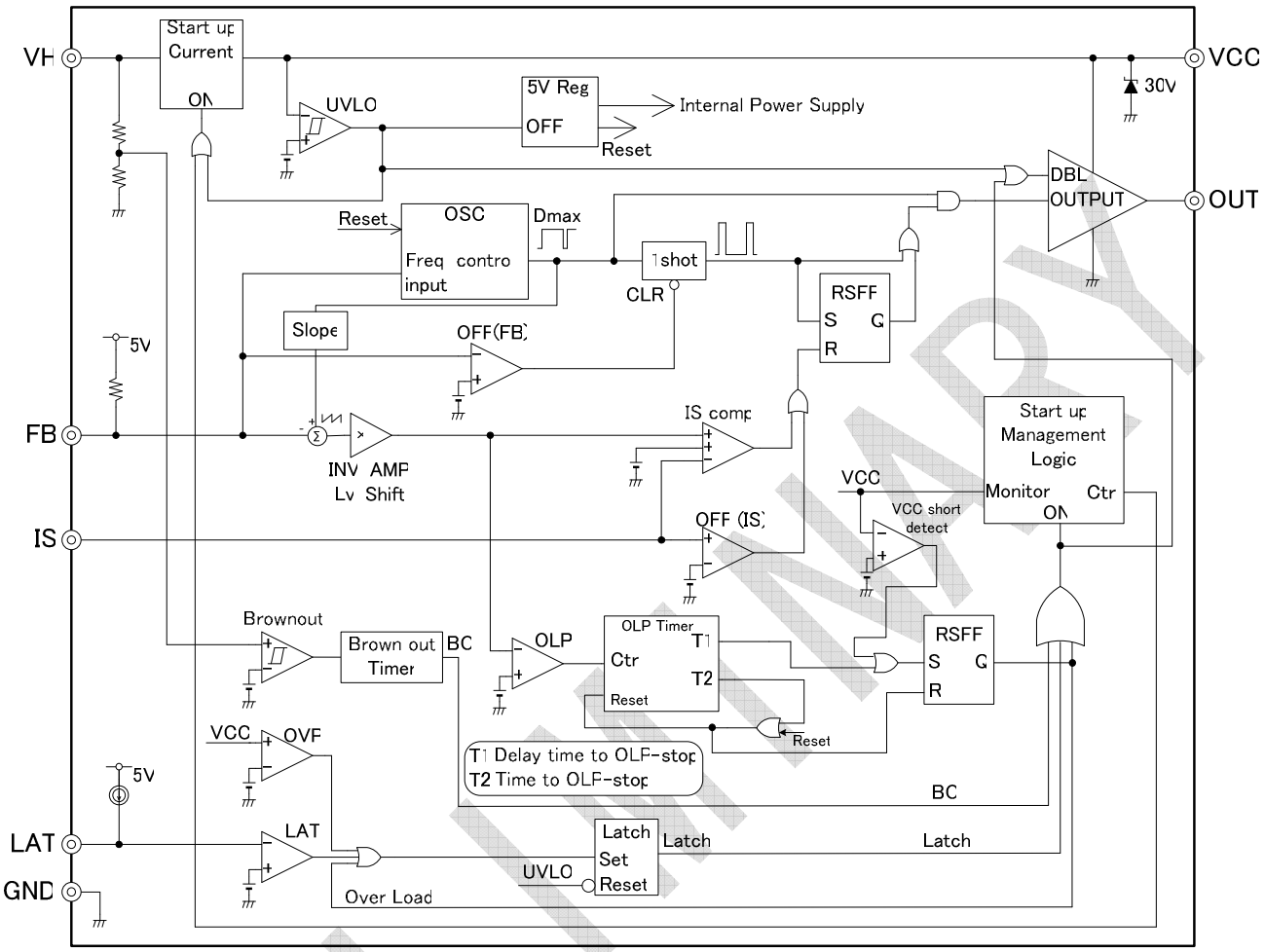
SOP-8



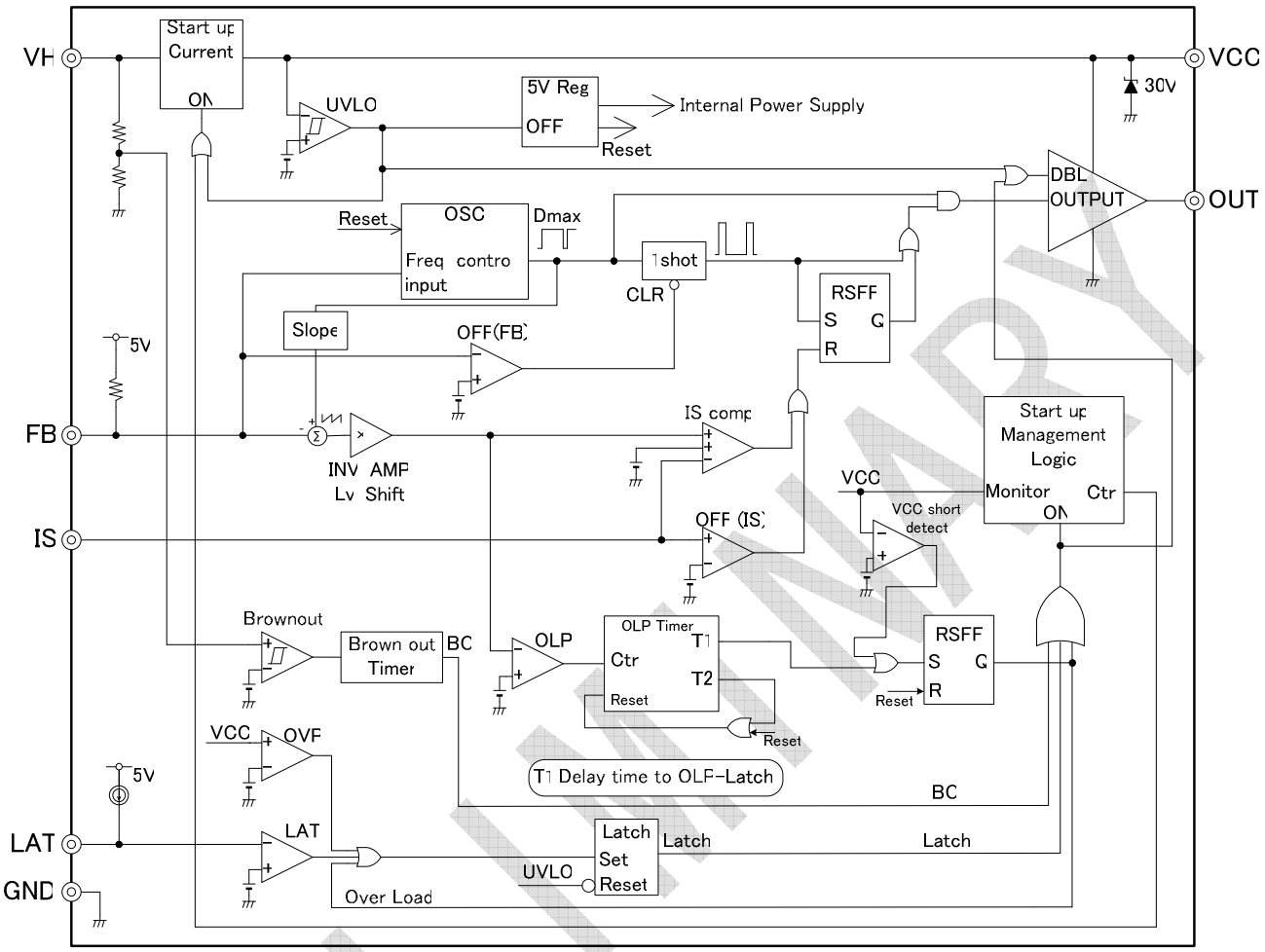
Unit:（mm）

4. Block diagram

FA5596(Overload protection : Auto recovery type)

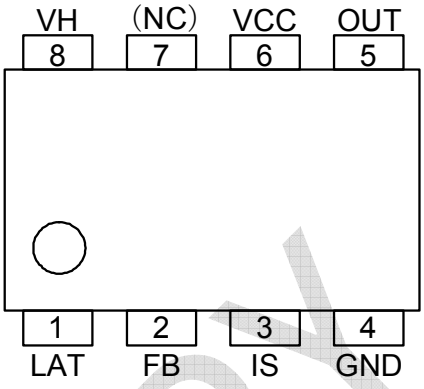


FA5597(Overload protection：Latch shutdown type)



5. Functional description of pins

Pin No.	Pin Name	Pin function
1	LAT	External latch signal input. Soft start.
2	FB	Feed back input. Light load and OLP detect
3	IS	Current sense (Input)
4	GND	Ground
5	OUT	Driver Output
6	VCC	Power supply
7	(NC)	(unused)
8	VH	High voltage input. Brown-out detect（750V max.）



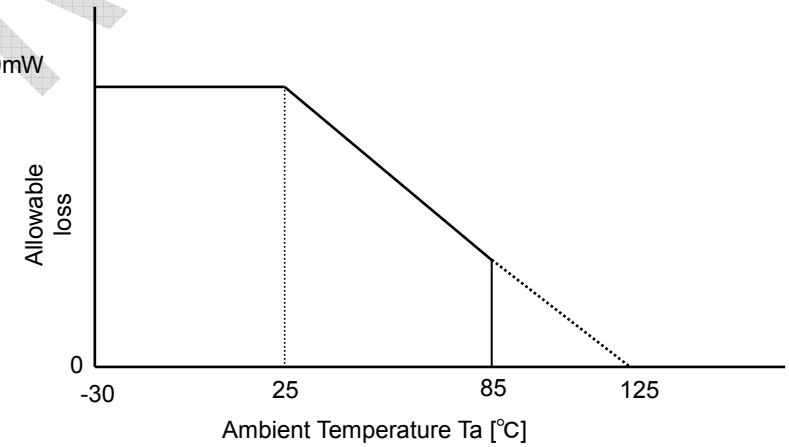
6. Rating & characteristics

"+" shows sink and "–" shows source in current prescription.

(1) Absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	VCC	28	V
OUT pin output peak current	Ioh	-0.5	A
	Iol	+1.0	A
OUT pin voltage	Vout	-0.3 to VCC+0.3	V
FB pin voltage	Vfb	-0.3 to 5.0	V
IS pin voltage	Vis	-2.0 to 5.0	V
LAT pin voltage	Vlat	-0.3 to 5.0	V
VH pin input voltage	Vvh	-0.3 to (750)	V
Total loss (Ta=25℃) (SOP)	Pd	400	mW
Junction temperature in operation	Tj	-30 to 125	℃
Storage temperature	Tstg	-40 to +150	℃

○Allowable loss reduction characteristics（SOP）



(2) Recommended operating condition

Item	Symbol	MIN	TYP	MAX	Unit
VCC Power supply voltage	VCC	11	18	24	V
High input voltage	Vvh	100		(650)	V
VH pin Resistance	Rvh	2		(10)	kΩ
LAT pin capacity	Clat	0.22	1.0	2.2	uF
VCC pin capacity	CVCC	10	33	100	uF
Operating ambient temperature	Ta	-30		85	℃

(3) Electric characteristics（in case nothing specified： Tj=25℃、VCC=18V）

Switching oscillator section （FB pin）

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Oscillation frequency	Fosc	FB=3V	(60)	65	(70)	kHz
Voltage stability	Fdv	VCC ： 10V to 24V	(-2)	—	(+2)	%
Temperature stability	Fdt	Tj= -30 to 125℃	(-5)	—	(+5)	%
Jitter range	Fm		(±5)	±7	(±9)	kHz
FB pin threshold voltage for light load mode	Vfbm		(1.7)	1.8	(1.9)	V
FB pin voltage at minmum frequency	Vfmin		(1.1)	1.2	(1.3)	V
Oscillation frequency reduction ratio	kf	Δf/ΔVfb	(80)	110	(140)	kHz/V
Minimum oscillation frequency	Fmin		(0.25)	0.45	(0.65)	kHz

External latch shutdown signal （LAT pin）

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Source current of LAT pin	ILAT	LAT=1.15V	(-80)	-70	(-60)	uA
Latch-off level	VthLAT		(1.00)	1.05	(1.10)	V
VthLAT/-ILAT *	RLAT		(13.5)	15	(16.5)	kΩ
Latch-off delay timer	TdLAT		(50)	65	(80)	us

* ; External resister (thermistor)

Soft start signal （LAT pin）

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Minimum pulse output voltage	Vss1	Start/Restart	(1.9)	2.1	(2.3)	V
Minimum pulse hold voltage	Vss2	Start/Restart	(2.3)	2.5	(2.7)	V
Soft start end voltage	Vss3		(1.5)	1.6	(1.7)	V

Pulse width modulation section （FB pin）

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Maximum duty cycle	Dmax	FB=4.5V	(75)	85	(95)	%
Minimum duty cycle	Dmin	FB=0V	—	—	0	%
Input threshold voltage	VthFB0	DUTY=0%	(340)	400	(460)	mV
FB pin source current	Ifb0	FB=0V	(-320)	-260	(-200)	uA

（ ）; provisional value

Over load protection (OLP) circuit section (FB pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Over load detection threshold voltage	VthFB			2.8		V
Over load detection Delay time	TdOLP	(VFB=4.5V)	(60)	70	(80)	ms
Waiting time of auto restart	TdOLP2	FA5596(VFB=4.5V)	(1300)	1530	(1760)	ms

Current sense section (IS pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Voltage gain	AvIS		(-4.6)	-3.8	(-3.0)	V/V
Maximum threshold voltage	VthIS1	VFB=4.5V	(-0.525)	-0.50	(-0.475)	V
Input bias current	IIS	VIS=0V	(-50)	-40	(-30)	uA
Minimum ON pulse width	Tmin1	Steady VH<220V **	(1400)	1700	(2000)	ns
	Tmin2	Steady VH>=220V **	(900)	1250	(1600)	
	Tmin3	Start/Restart / OLP	(180)	280	(380)	
Delay to output	TpdIS	Tj=25℃	(100)	200	(300)	ns

** ; Tmin2 → Tmin1(If VH voltage is DC input)

VCC circuit section (VCC pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Start-up threshold voltage	VCCon		(16)	18	(20)	V
Shutdown threshold voltage	VCCoff		(8)	9	(10)	V
Hysteresis width	Vhys		(7)	9	(11)	V
VCC over-voltage protection threshold voltage	Vthovp		(25)	26	(27)	V
Short circuit detection voltage	Vthshort		(10)	11	(12)	V

Output circuit section (OUT pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Low output voltage	VOL	IOL=100mA, VCC=18V	(0.4)	0.8	(1.6)	V
High output voltage	VOH	IOH= -100mA, VCC=18V	(14.5)	16	(18)	V
Rise time	tr	CL=1nF	(30)	60	(100)	ns
Fall time	tf	CL=1nF	(20)	40	(70)	ns

( ) ; provisional value

High-voltage input section (**VH pin、VCC pin**)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Current of VH pin	IHrun	VH=450V, VCC>VCCon	(60)	100	(140)	uA
	IHstb	VH=120V, VCC=0V, Tj=25℃	(3.5)	6.5	(9.5)	mA
Threshold voltage level at brown-out (VH pin)	VthBO	VH pin=decreasing	(89)	99	(109)	V
Threshold voltage level at Brown-in (VH pin)	VthBI	VH pin=increasing	(95)	105	(115)	V
Brown out delay time	TpdBO	FA5596/97	(30)	50	(70)	ms
VCC voltage at Latch	VCCLHH	VH=120V, 1time clamp	(13)	14.5	(16)	V
	VCCLH	VH=120V, Upper ﾚﾍﾞﾙ	(12)	13	(14)	
	VCCLL	VH=120V, Lower ﾚﾍﾞﾙ	(11)	12	(13)	
VCC voltage at Brown-out/OLP	VCCclp3	VCC rising	(14)	15	(16)	V
	VCCclp4	VCC falling	(12)	13	(14)	
Charge current for VCC pin	Ipre1	VCC=16V, VH=120V	(-14)	-8	(-3.5)	mA
	Ipre2	VCC=11V, VH=120V, ﾗｯﾁ時	(-18)	-12	(-6)	

Power supply current (**VCC pin**)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Operating-state supply current	ICCop1	Duty cycle=Dmax FB=2V、OUT=No Load	(1.0)	1.4	(1.7)	mA
	ICCop2	Duty cycle=0% FB=0V	(0.95)	1.35	(1.65)	mA
Latch mode supply current	ICClat	FB=open, VCC=11V	(600)	900	(1100)	uA
Supply current at Brownout/OLP	ICCbo	FB=open, VCC=18V	(600)	900	(1100)	uA
VCC pin zenner clamp voltage	VCCzd	Iz=2mA	(28)	30	(34)	V

( ) ; provisional value

8. Operation of each block

(1) Startup circuit

The IC integrates a startup circuit having withstand voltage of 750V to achieve low power consumption.
Fig.1 to Fig.3 show connections.
Turning on the power, capacitor C2 connected to the VCC terminal is charged and the voltage increases due to the current fed from the startup circuit to the VCC terminal. If the ON threshold voltage (Vcc = 18V typ) of the under-voltage lockout circuit (UVLO) is exceeded, the power for internal operation is turned on, and the IC starts operating.
The current supplied from the VH terminal to the VCC terminal is approximately 6.5mA(Typ.) when VCC = 0V. As the VCC voltage increases, the supply current decreases.
A resister of 2kΩ is connected in series to the VH terminal for short-circuit protection of the VCC terminal.

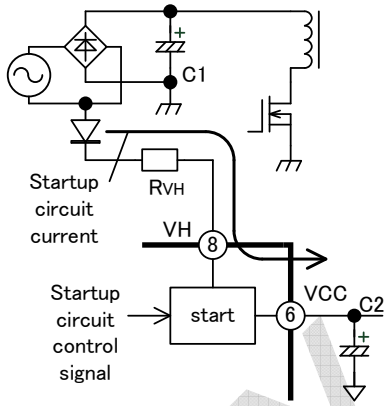


Fig.1 Startup circuit 1 (Half-wave)

Fig.1 shows a typical connection where the VH terminal is connected to the half-wave rectifier circuit of AC input voltage.
The startup time of this connection is the longest in 3 types of connection.

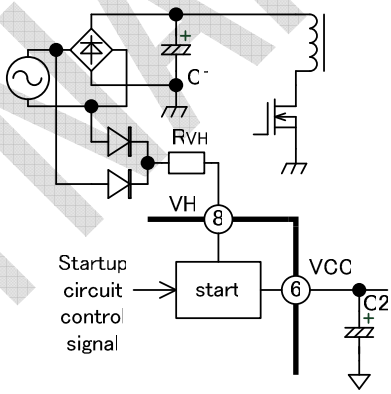


Fig.2 Startup circuit 2 (Full-wave)

Fig.2 shows the connection where the VH terminal is connected to the full-wave rectifier circuit of AC input voltage. The startup time of this connection is approximately half of the connection shown in Fig.1.

Fig.3 shows the connection where the VH terminal is connected to the back of rectification and smoothing of AC input voltage. The startup time of this connection is the shortest in 3 types. In this connection, however, even if the AC input voltage is shut down after the IC enters the latch mode, the voltage charged in C1 is kept impressed to the VH terminal, requiring much time for the latch mode to be reset. It takes approximately several minutes to reset the latch mode, although the time varies depending on conditions.

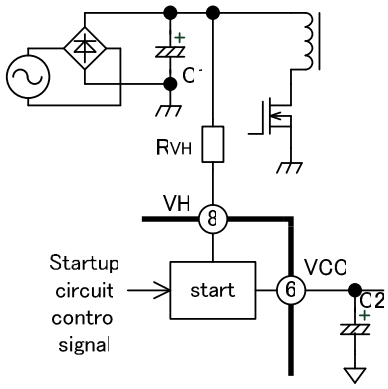


Fig.3 Startup circuit 3 (Rectification)

If the VCC terminal voltage exceeds the ON threshold voltage(VCCon=18V (typ)) and the IC starts operating, the startup circuit is shut down and the VH terminal current decreases to several 10 to several 100uA.

After the startup, the IC goes into switching operation, and is operated with the power supplied from the auxiliary winding. If the overload or overvoltage protection is actuated, causing the IC to enter the latch mode, then the startup circuit is subjected to ON/OFF control to maintain the VCC voltage within the 12V to 13V (typ) range.

(2) Oscillator

This oscillator is used to determine the switching frequency. The switching frequency in the normal operation mode is set to 65kHz (typ) within the IC.
To minimize the loss of power in the standby state, this IC is equipped with a function of automatically decreasing the switching frequency under light load.
When the FB terminal voltage decreases down to 1.7V (typ) or lower under light load, the frequency decreases almost linearly proportional to the FB terminal voltage.(See Fig.4)
The minimum frequency, Fmin, has been set to 0.45kHz (typ).
When the load further decreases and thus the FB terminal voltage decreases down to 0.4V (typ) or lower, the switching is stopped. (See one-shot circuit.)
In addition to trigger signals for determining switching frequency, the oscillator generates pulse signals for determining the maximum duty cycle and ramp signals for performing slope compensation.

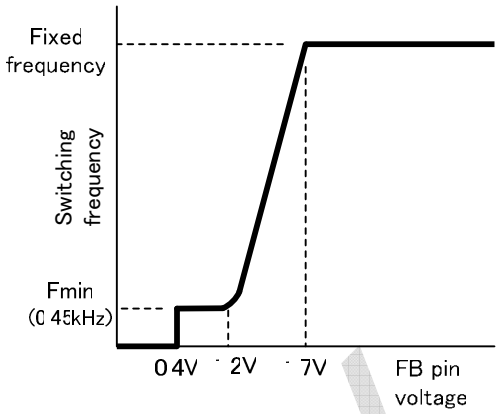


Fig.4 Oscillation frequency

(3) Current comparator & PWM latch circuit

The IC performs current mode control. Fig.5 shows a circuit block for basic operations, and Fig.6 shows a timing chart.
The polarity of the current detection voltage of the IS terminal is negative. The GND of the IC is connected between the current detection resistor Rs and the MOSFET. (See Fig.5)

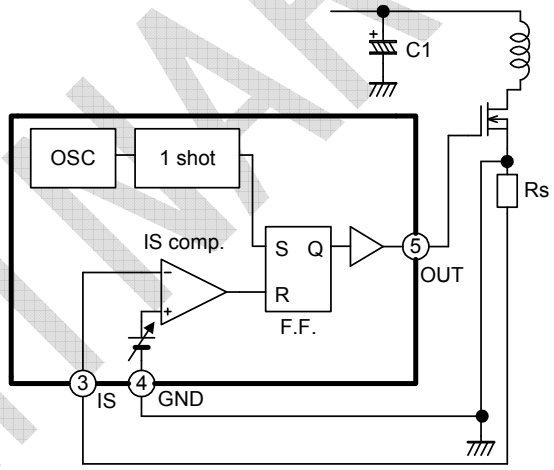


Fig.5 Current mode basic operation circuit block

A trigger signal having the switching frequency that is output from the oscillator is input to the PWM latch (F.F.) through the one-shot circuit as a set signal. Then the output of the PWM latch as well as the OUT terminal voltage reaches the High state.
On the other hand, the current comparator (IS comp.) monitors the MOSFET current, and if the threshold voltage is reached, a reset signal is output. When a reset signal is input, the output of PWM latch (F.F.) as well as the OUT terminal voltage reaches the Low state.
The ON pulse width of the OUT terminal is thus controlled with the threshold voltage of the current comparator (IS comp.).
The output is controlled by changing the threshold voltage of this IS comp. with feedback signals.

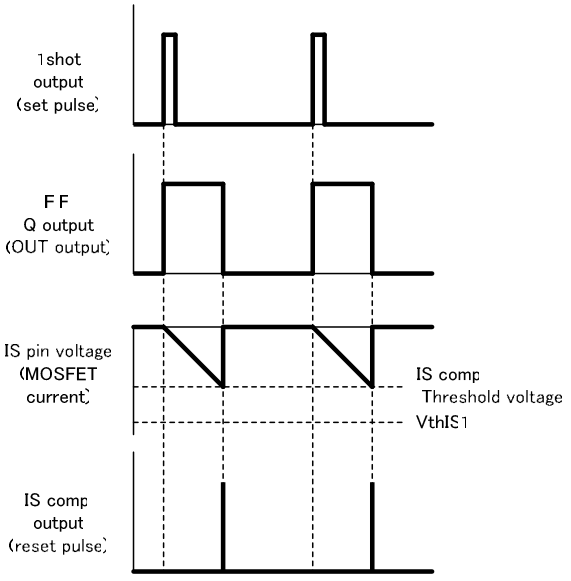


Fig.6 Current mode basic operation timing chart

As shown in Fig.7, the FB terminal voltage is level-shifted by a reverse amplifier and input into the current comparator (IS comp.) as the threshold voltage. In addition, -0.5V (typ) reference voltage is input inside the IC to regulate the maximum input threshold voltage of the IS terminal, VthIS1 (overcurrent control threshold).
The reverse amplifier output or the maximum IS terminal input threshold voltage, VthIS1, whichever is higher, is given precedence as the IS terminal threshold voltage.
(Example: When the output of the reverse amplifier is -0.2V in a product whose maximum threshold voltage of the IS terminal, VthIS1, is -0.5V, the output of the reverse amplifier is given precedence and thus the current comparator is reversed when the IS terminal voltage reaches -0.2V.)

In normal operation, the output voltage of the power supply is maintained constant by changing the threshold voltage of the current comparator via the FB terminal voltage.
When the output voltage decreases, the feedback circuit increases the FB voltage to allow the threshold voltage of the current comparator to scale out to Low, thus increasing the MOSFET current.
The maximum input threshold voltage of the IS terminal, VthIS1 (-0.5V typ) controls the maximum current of the MOSFET. If the FB terminal voltage increases under overload, the output of the reverse amplifier scales out to Low, decreasing down to lower than VthIS1. The threshold voltage of the IS terminal is thus controlled not to exceed VthIS1.
The oscillator outputs pulses for determining the maximum duty cycle. Using these pulses, the maximum duty cycle has been set to 85% (typ).

(4) One shot circuit (minimum ON width)

When the MOSFET is turned on, a surge current is generated due to discharge corresponding to the capacitance of the main circuit and gate drive current. If this surge current reaches the IS terminal threshold voltage, the current comparator output is reversed, and consequently normal pulses may not be generated from the OUT terminal.
To avoid this phenomenon, a minimum ON width of OUT terminal output is set within the one-shot circuit block of the IC.
If a trigger signal having the switching frequency is input from the oscillator, a pulse having a specific width is output as a PWM latch (F.F.) set signal.
Since the set signal has priority over the input signal of the PWM latch, the output of the PWM latch (F.F.) is not reversed while the set signal from the one-shot circuit is being input, even if a reset signal is input from the current comparator (IS comp.) (See Fig.5)
As a result, the input to the IS terminal is kept invalid for the specified period of time immediately after the output pulse is generated from the OUT terminal (minimum ON width), and made not to respond to the surge current at turn-on. (See Fig.8)
This minimum ON width function eliminates the need of a noise filter for the IS terminal in principle.
The minimum ON width is usually set to 1250ns or 1700ns (typ) in normal operations, and to 280ns (typ) at startup or rebooting to prevent the transient MOSFET drain voltage from surging.

In addition, an exclusive comparator is integrated to keep the output pulse at zero under no load. (See Fig.9)
This comparator reverses its output when the FB terminal voltage decreases down to 400mV (typ), preventing a set pulse to be input to the PWM latch (F.F.). The output is thus maintained in Low state and switching is stopped.

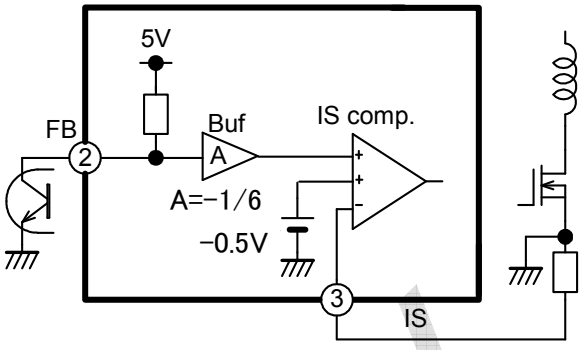


Fig.7 Current comparator

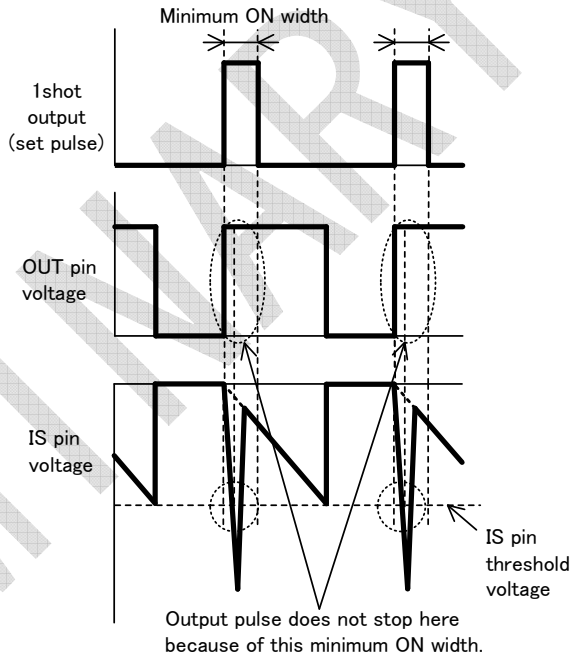


Fig.8 Minimum ON width

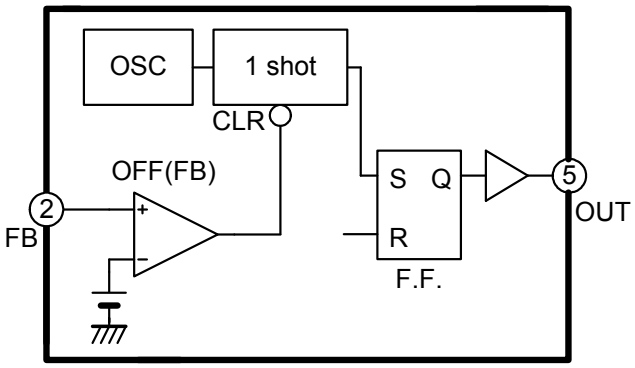


Fig.9 Output shutdown function of FB pin

(5) Overload protection circuit

(5-1) Latch type

FA5597 integrates overload protection of the latch mode. Fig.10 shows a circuit block and Fig.11 shows a timing chart of protecting operation.

An overload state is detected by negative voltage of the IS terminal. If the peak voltage of the pulsing IS terminal 70 ms continuously exceeds the threshold voltage VthFB = 2.8 V, it is judged to be in an overload state and the mode is switched to the latch mode. Overload latch delay time (70 ms) is fixed inside the IC.

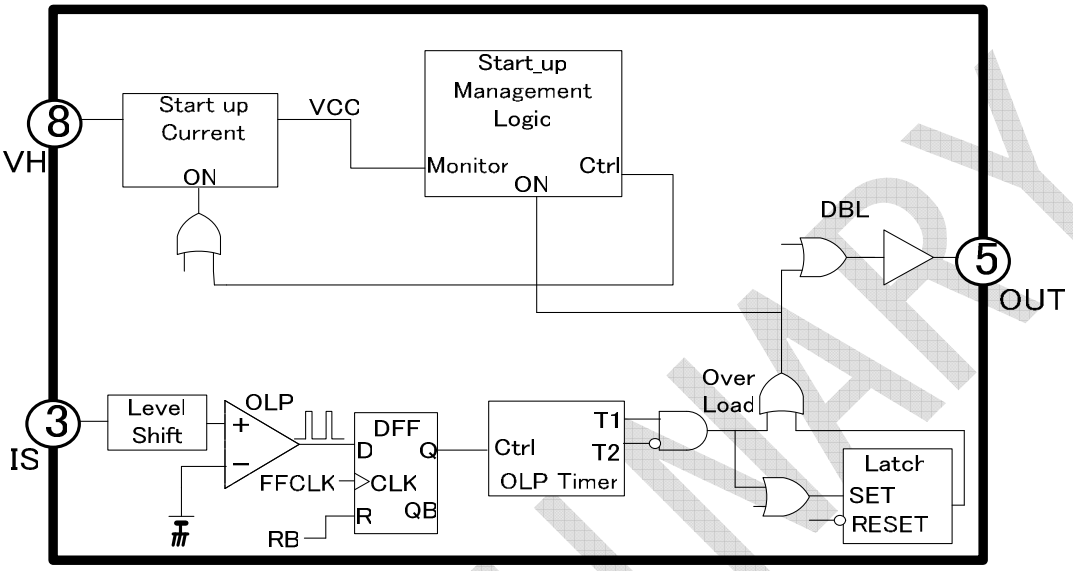


Fig.10 Overload protection circuit (latch)

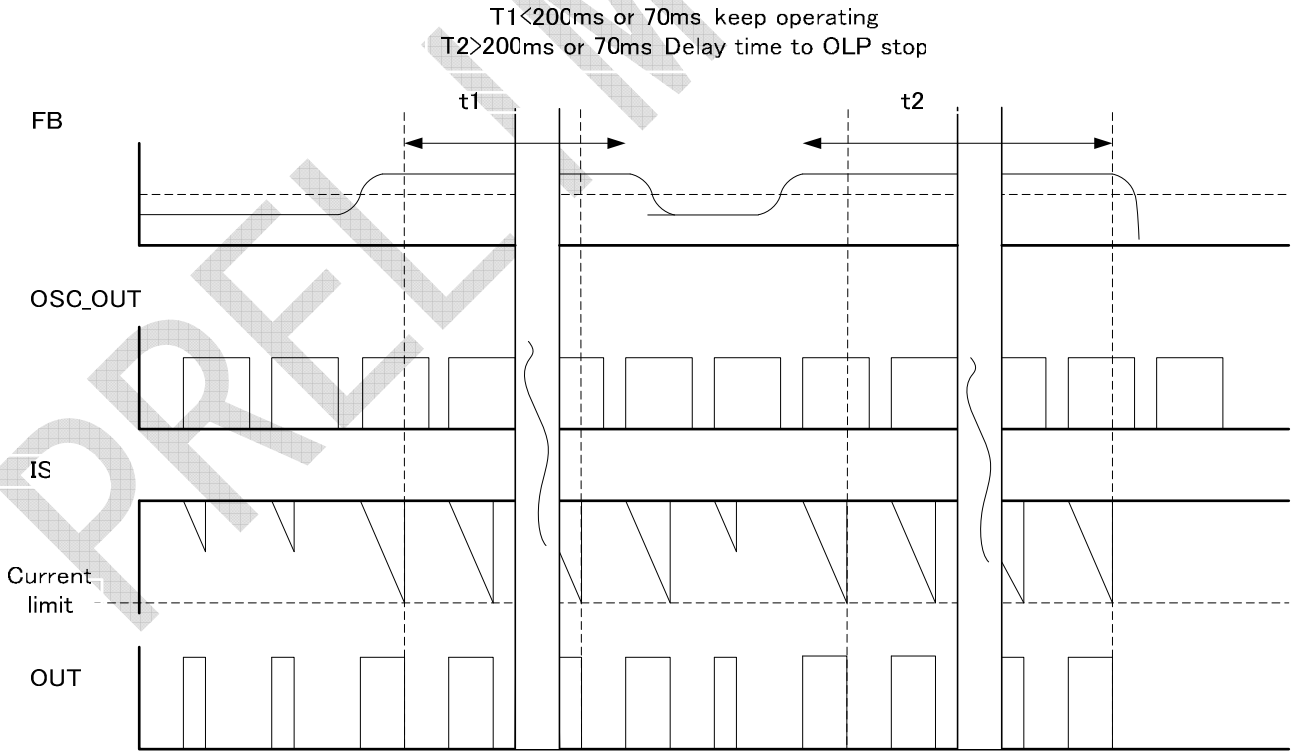


Fig. 11 Overload protection timing chart (latch)

(5-2) Auto restart type

FA5596 integrates overload protection of the auto recovery mode. Fig.12 shows a circuit block and Fig.13 shows a timing chart of protecting operation.

An overload state is detected by negative voltage of the IS terminal. If the terminal peak of the pulsing IS voltage 70 ms continuously exceeds the threshold voltage VthFB = 2.8V, it is judged to be in an overload state and the switching is stopped. Auto recovery is performed after 1530 ms elapse. These periods of time are fixed inside the IC.

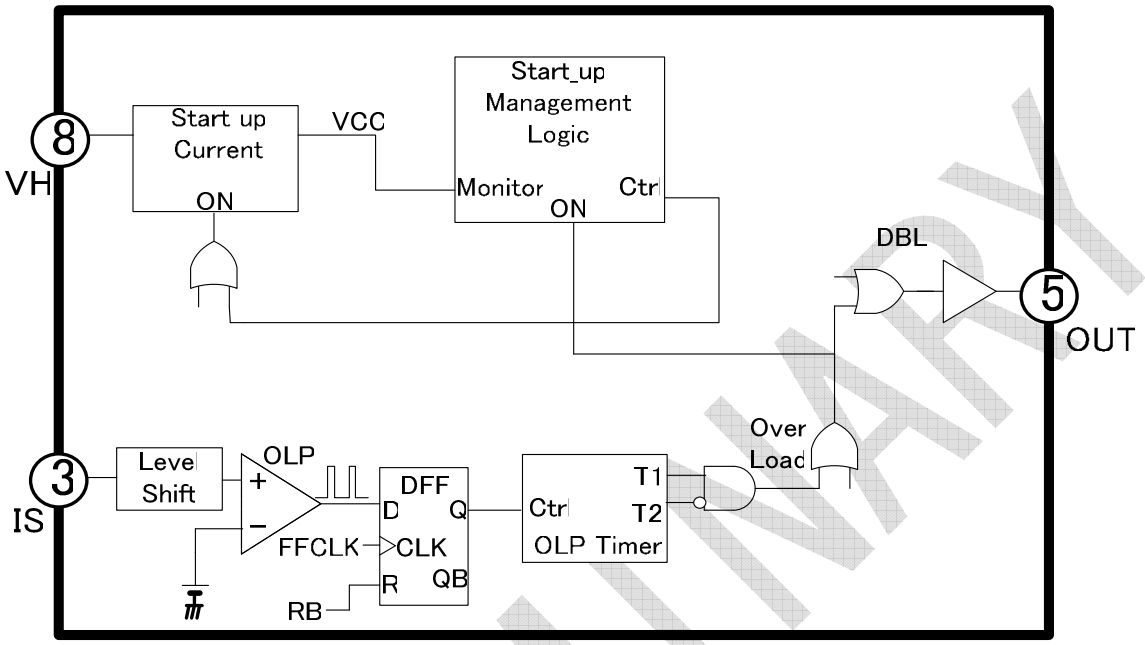


Fig.12 Overload protection circuit (auto recovery)

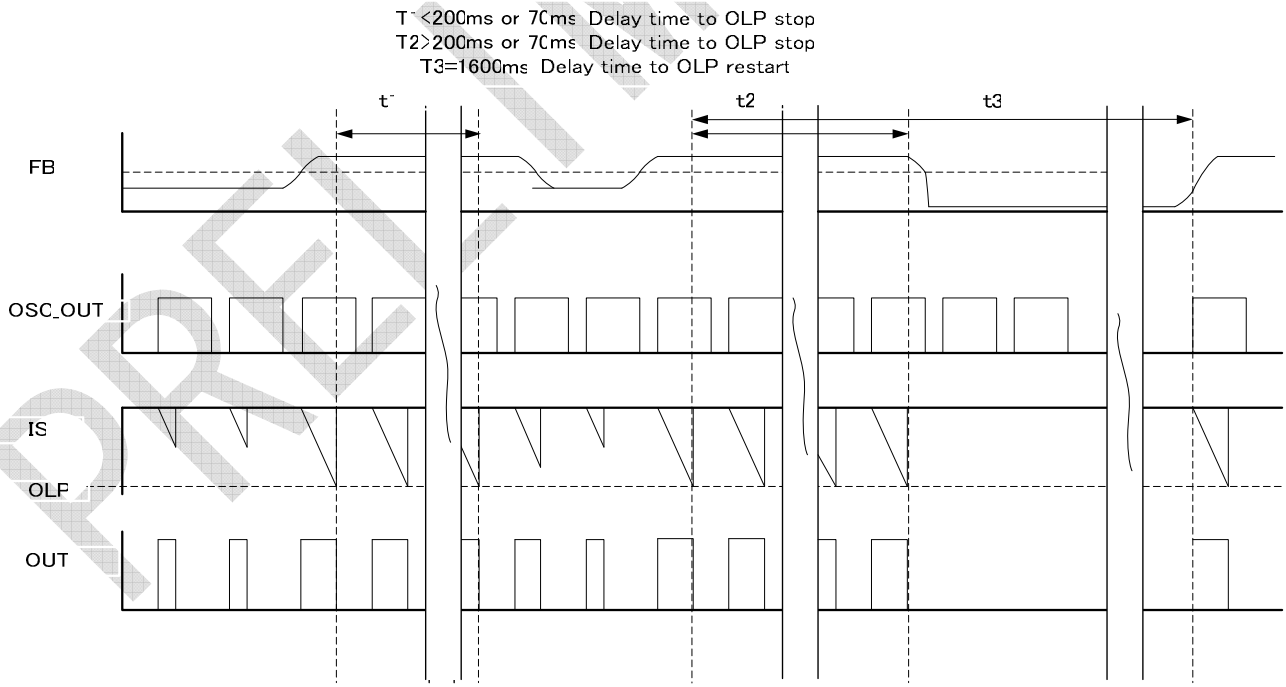


Fig. 13 Overload protection timing chart (auto recovery)

(6) Overvoltage protection circuit (VCC terminal)

The IC integrates an overvoltage protection circuit for monitoring the VCC terminal voltage. (See Fig.14)
If the VCC voltage increases and exceeds 26V typ, which is the reference voltage of the comparator (OVP), the comparator output is reversed to High level, setting the latch circuit to perform latch shutdown.
At this time, the startup circuit is subjected to ON/OFF control to maintain the latch mode, thus keeping the VCC voltage within the 12V or 13V (typ) range.
To cancel the latch mode, shut down the input voltage to cause brownout, as in the case of the overload protection.(latch type)
Since 65μs (typ) delay time has been set to the set input of the latch circuit, the latch mode is not entered even if the VCC terminal exceeds the detection voltage temporarily.

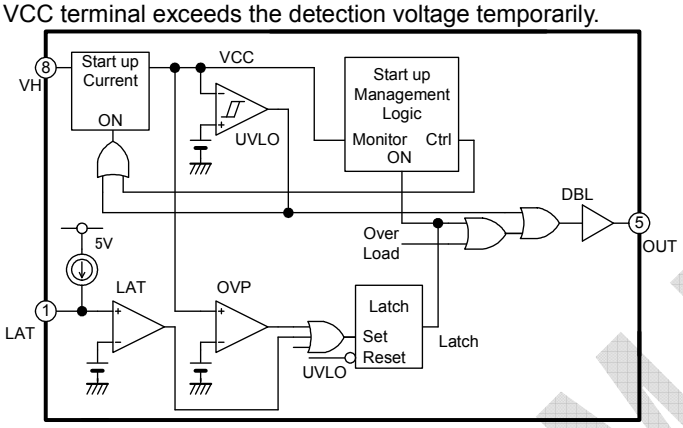


Fig. 14 Overvoltage protection circuit

(7) Latch shutdown circuit by an external signal

The LAT terminal is equipped with a latch shutdown function. (See Fig.15)
By decreasing the LAT terminal voltage to 1.05V or lower, the IC enters the latch mode.
To cancel the latch mode, shut down the input voltage to cause brownout, as in the case of the OVP. (former section)

If the external latch shutdown function by the LAT terminal is not to be used, connect a capacitor only.

Connect an NTC thermistor to the LAT terminal to use the overheat protective function. (See Fig.15)

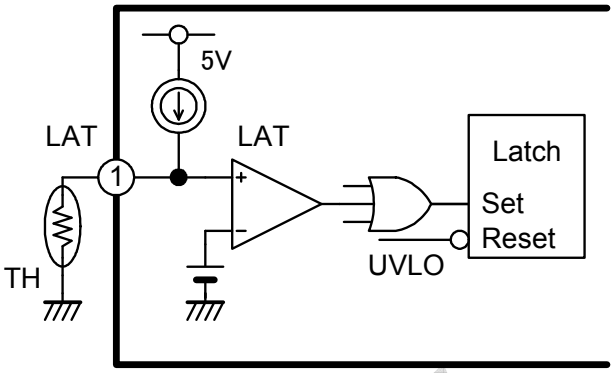


Fig. 15 Overheat protection function using a thermistor

(8) Undervoltage lockout circuit (VCC terminal)

The IC integrates an undervoltage lockout (UVLO) function to prevent circuit malfunction that might occur when power supply voltage decreases. When the VCC voltage increases from 0V and reaches 18V (typ), the circuit starts operating. When the VCC decreases down to 9V (typ), the circuit stops operating.
In a state in which the undervoltage lockout function is actuated to stop IC operation, the OUT terminal is forcibly made to enter the Low state. The latch mode of the protection circuit is also reset.

(9) Output circuit

The push/pull structure output circuit drives the MOSFET directly. The peak output current of the OUT terminal is 0.5A (source) and 1.0A (sink) in the maximum absolute ratings.
In a state in which the IC is stopped in the undervoltage lockout circuit or operation is suspended in the latch mode, or in an auto reset wait state by overload protection function, the OUT terminal is brought into the Low level, and the MOSFET is interrupted.

(10)Short circuit detection

If reduction of the VCC voltage (Vthshort = 12 V) is detected during short circuit, FA5596/FA5597 stop the operation regardless of the over load timer time (200 ms or 70 ms)

(11)Frequency diffusion（Spread spectrum）

FA5596/FA5597 perform frequency modulation of ± 4.5 kHz for switching frequency 65 kHz (during the operation in which the FB terminal voltage is higher than 1.7 V.). This function enables more noise energy of the switching to disperse compared to the case with fixed frequency and obtains a conduction EMI reduction effect. While the reduction effect depends on the filter parts mounted on the power supply board, effective use of this function allows the reduction of the number of the filter parts and the constants.

(12) Brownout

The VH waveform in Fig.16 shows the input half-wave of the VH terminal. If its peak voltage reaches the brownin threshold voltage level, brownin is detected and operation is started. The voltage is reduced to 0 V in every cycle because of the half-wave input and the timer for the brownout delay time counts. Since the brownout delay time longer than the half-wave cycle is set, a brownout state is not caused during the reduced half-wave. However, if the VH terminal voltage is reduced by the brownout threshold voltage and then the brownout delay time elapses, a brownout shutdown state occurs.
Fig. 17 shows oscillation frequency dependence of the brownout delay time.

Since the number of count is fixed, the clock cycle and the brownout delay time become longer at lower oscillation frequency on light load.

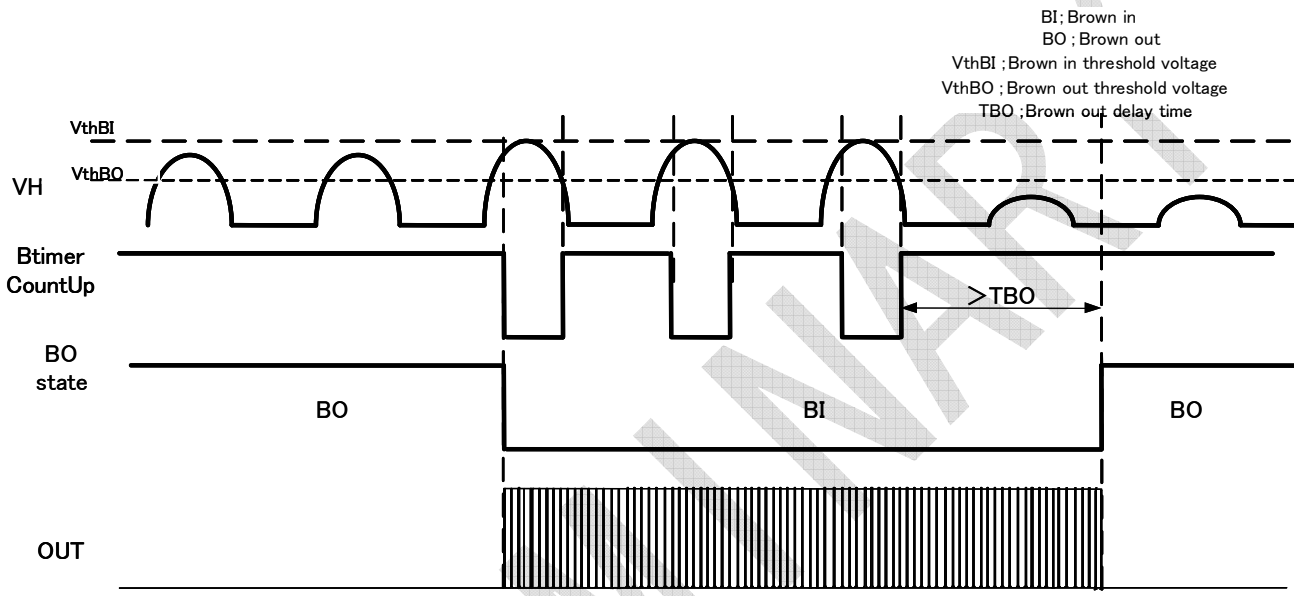


Fig.16 Brownout operation

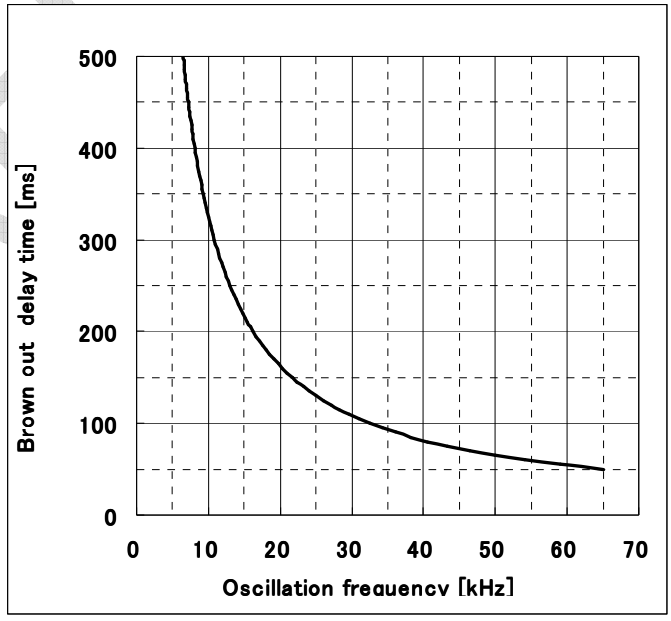


Fig.17 Brownout delay time

(13) Soft-start

Fig. 18 shows the soft-start operation. The BO signal is a brownout signal and becomes H during brownout and L during brownin. See 8-(12) for the description of the LAT terminal operation. The following is the calculation method for the soft-start.

Areas ① to ③ show the LAT terminal waveform at startup. Area ③ is the soft-start period in which the pulse width is gradually increased (the period of the LAT terminal voltage of 2.0 V to 1.75 V).

① ② The period in which the LAT terminal voltage is reduced from 2.4 V to 2.0 V is the output period of the minimum ON width (The LAT terminal voltage is discharged at a constant current of 70 uA.)

③ Effective soft-start period in which the pulse width is gradually increased (The LAT terminal voltage is discharged at a constant current of 70 uA.)

④ Dmax (maximum input threshold voltage operation)

⑤ Start of PWM operation

Since the voltage is discharged at a constant current of 70 uA (typ) in areas ① to ③, a discharge time is calculated by T = (C*V)/ILAT

Area ② is an effective soft-start period. The voltage difference and the discharge current are set in the IC. When ΔV = (2.0 – 1.5) V = 0.5 V and ILAT = 70 uA, if CLAT=1 uF, the effective soft-start period is T = (C*V)/ILAT = (1 uF*0.5 V)/70 uA = 7.1 ms

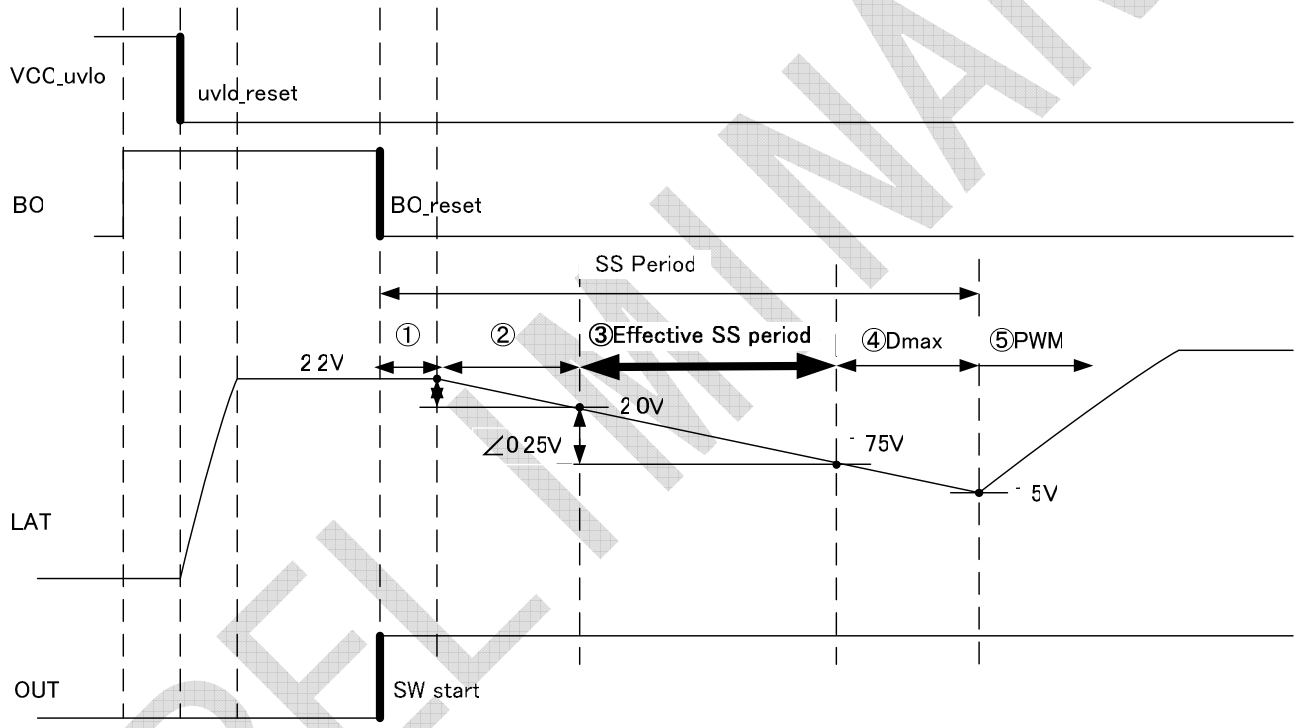


Fig.18 Soft-start operation

9. Advice for designing

(1) Startup

To properly start or stop the power supply, a capacitor having appropriate capacitance must be selected.
Fig.19 shows the VCC voltage at the time of startup when an appropriate capacitor is connected.
When the power is turned on, the capacitor of the VCC is charged with the current supplied from the startup circuit, and the voltage increases.
When the VCC reaches the ON threshold voltage, the IC starts operating. The IC is operated based on the voltage supplied from the auxiliary winding. Note that during the period immediately after startup until the voltage of the auxiliary winding starts up, the VCC decreases. Select a capacitor for the VCC that does not allow the VCC to decrease down to the OFF threshold voltage.
Specifically, a VCC terminal capacitor whose OFF threshold voltage is 11V or higher is recommended.

If the capacitance of the VCC terminal is too small, VCC decreases to lower than the OFF threshold voltage before the voltage of the auxiliary winding starts up as shown by Fig.20. In this case, the VCC repeats up/down operation between ON and OFF threshold voltages, and consequently the power supply cannot be turned on.

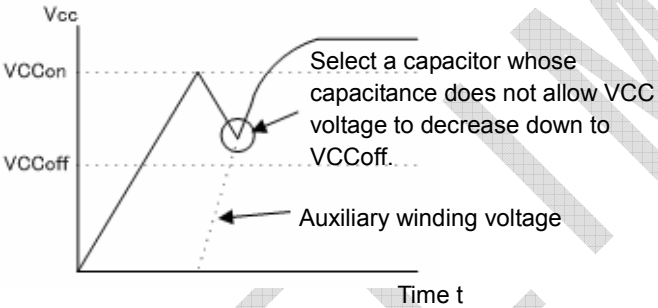


Fig. 19 VCC terminal voltage at startup

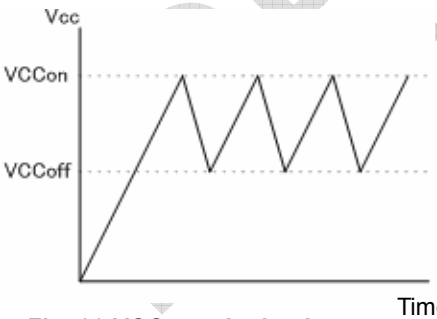


Fig. 20 VCC terminal voltage at startup (when capacitance is too small)

(2) VCC hold time

To prevent the VCC terminal voltage from decreasing to lower than the UVLO OFF threshold voltage due to sudden load change and other reasons, it may be desirable that the capacitance of the capacitor to be connected to the VCC terminal be made larger.
However, if the capacitance of the capacitor of the VCC terminal is increased, the startup time is made longer.
In such cases, the circuit shown in Fig.21 can balance the capacitance and the startup time.
By setting C1 to less than C2, the startup time can be kept short. Since current is supplied via C2 after startup, the VCC terminal voltage hold time can be kept long even under sudden change conditions.

(3) Gate drive circuit

To adjust switching speed and prevent vibration of the gate terminal, a resistor is connected between the MOSFET gate terminal and the OUT terminal of the IC in general.
In some cases, driving current for turning on the MOSFET and that for turning it off are required to be determined separately.
In this case, connect a gate drive circuit shown in Fig.22 or 23 between the gate terminal of the MOSFET and the OUT terminal.

In Fig.22, the current is limited by R1 and R2 when the power is turned on, while the current is limited only by R2 when it is turned off.
In Fig.23, the current is limited only by R1 when the power is turned on, while the current is limited by R1 and R2 connected in parallel when the power is turned off.

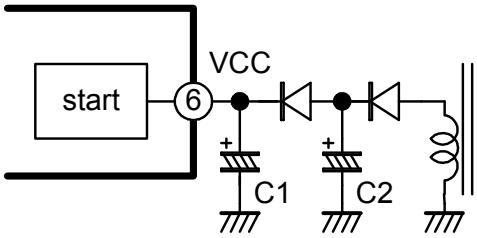


Fig. 21 VCC circuit

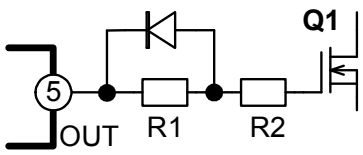


Fig. 22 Gate drive circuit (1)

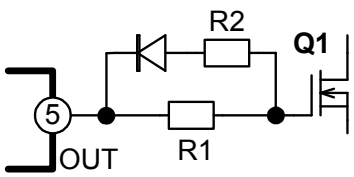


Fig. 23 Gate drive circuit (2)

(4) LAT terminal

• To perform overheat protection using an NTC thermistor

As shown in Fig.15, thermistor TH1 is connected to the LAT terminal to perform overheat protection (latch shutdown). Since the LAT terminal source current is 70μA (Typ.), select TH1 whose resistor Rth satisfies the following expression at the desired overheat protection temperature. If temperature setting for overheat protection is not feasible with TH1 only, connect an additional resistor in series for adjustment.

$$Rth \leq 1.00V / 70\mu A \approx 15k\Omega$$

• To perform latch shutdown using an independent abnormality detection signal

To perform latch shutdown with an external signal, connect a peripheral circuit, allowing the LAT terminal voltage to be kept below 1.0V. Fig.24 shows a typical circuit connection.

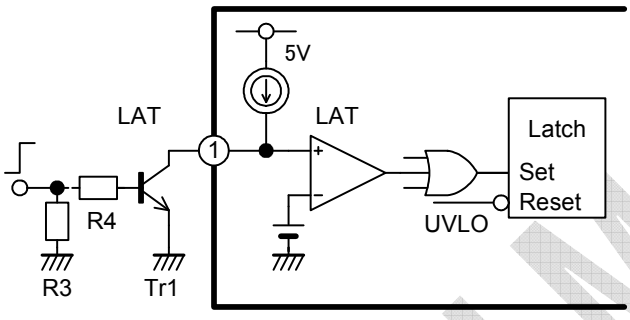


Fig. 24 Latch shutdown function by an external signal

(5) Feedback

Fig.25 shows the circuit configuration of the FB terminal.
A photo-coupler PC is connected as a feedback circuit that monitors the output voltage and performs PWM control.

This signal gives threshold voltage for the current comparator. Consequently, if noise is added to this signal, the output pulses are disturbed. Capacitor C4 is generally connected for protection against noise.

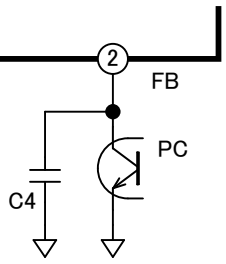


Fig. 25 FB terminal circuit configuration

(6) Current sensing unit

As described in 8-(4) One-shot circuit, the minimum ON width is set for this IC to minimize malfunction due to surge current that occurs when the power MOSFET is turned on. However, if the surge current that occurs at the time of power ON is large, or noise is applied externally at the time of power ON, malfunction might occur.
In such cases, add RC filters C6 and R7 as shown in Fig.26. To ensure efficient operation of the capacitor C6, place it as close to the IC as possible, and lay wiring with extreme care.

(7) Improvement of input power at light load

The IC integrates the function of reducing standby power consumption by lowering oscillation frequency under light load.
However, since load conditions vary depending on the power supply setting, the settings within the IC may be insufficient to reduce standby power consumption.
In such cases, connect resistor R8 as shown in Fig.27 to reduce oscillation frequency.
Since the input impedance of the IS terminal is about 100kΩ, resistor R8 shall be several 100kΩ to MΩ.
As shown in Fig.28, by connecting the resistor between the OUT terminal and the IS terminal, the same light-load correction effect can be obtained and in addition, the loss of resistor R8 can be reduced compared to the case in which it is connected to the VCC terminal.

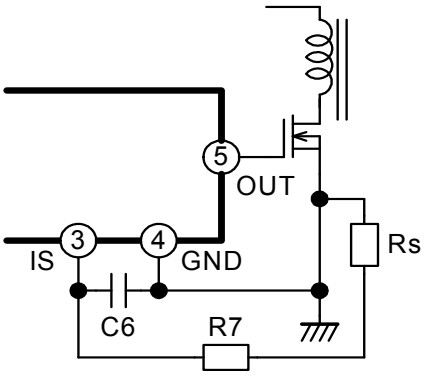


Fig. 26 IS terminal filter

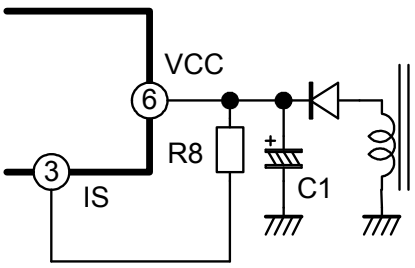


Fig. 27 Correction circuit for improvement of input power under light load(1)

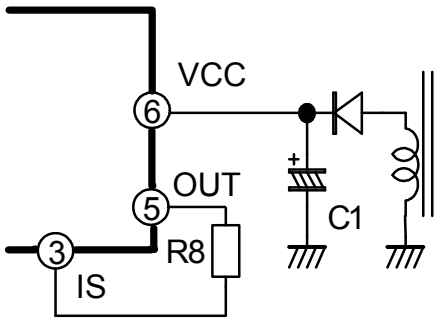


Fig. 28 Correction circuit for improvement of input power under light load(2)

(8) Reduction of dependency of overload detection level on input voltage

Since the gradient of the inductor current of a transformer varies depending on the input voltage in the overload protection function, the current value determined to be overload also varies. The higher the input voltage, the higher the output current that causes overload shutdown to occur.

As shown in Fig.29. resistor R9 can be connected between the auxiliary winding and the IS terminal to minimize the dependency of the overload detection level on input voltage (IS terminal line correction).

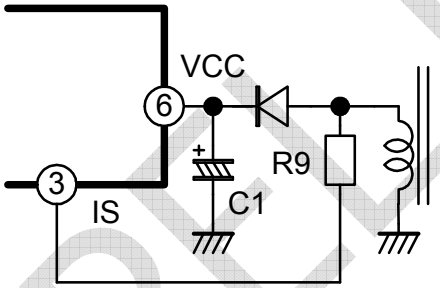


Fig. 29 Reduction of dependency of overload detection level on input voltage

(9) Prevention of malfunction due to negative potential of the terminal

If large negative voltage is applied to each terminal of the IC, the parasitic element within the IC may be actuated, thus causing malfunction to occur. Be sure to maintain the voltage to be applied to each terminal within the maximum absolute ratings.

(10) Loss calculation

To use the IC within its ratings, the loss of the IC may have to be found. However, it is not feasible to measure loss directly. The following is an example of finding a rough value of loss by calculation.

The rough value of the total loss of the IC, Pd, can be calculated using the following expression:

$$Pd \fallingdotseq VCC \times (ICCop1 + Qg \times fsw) + VVH \times IHrun$$

where,
VVH: voltage to be applied to the VH terminal,
IHrun: current fed to the VH terminal during operation,
VCC: power voltage,
ICCop1: Consumption current of the IC
Qg: electrical charge to be input to the MOSFET gate used, and
Fsw: switching frequency.

A rough value can be found using the above expression, and the total loss found by the calculation, Pd, is slightly larger than the actual value.
Be sure to take into consideration that each characteristic value varies depending on temperatures and other factors.

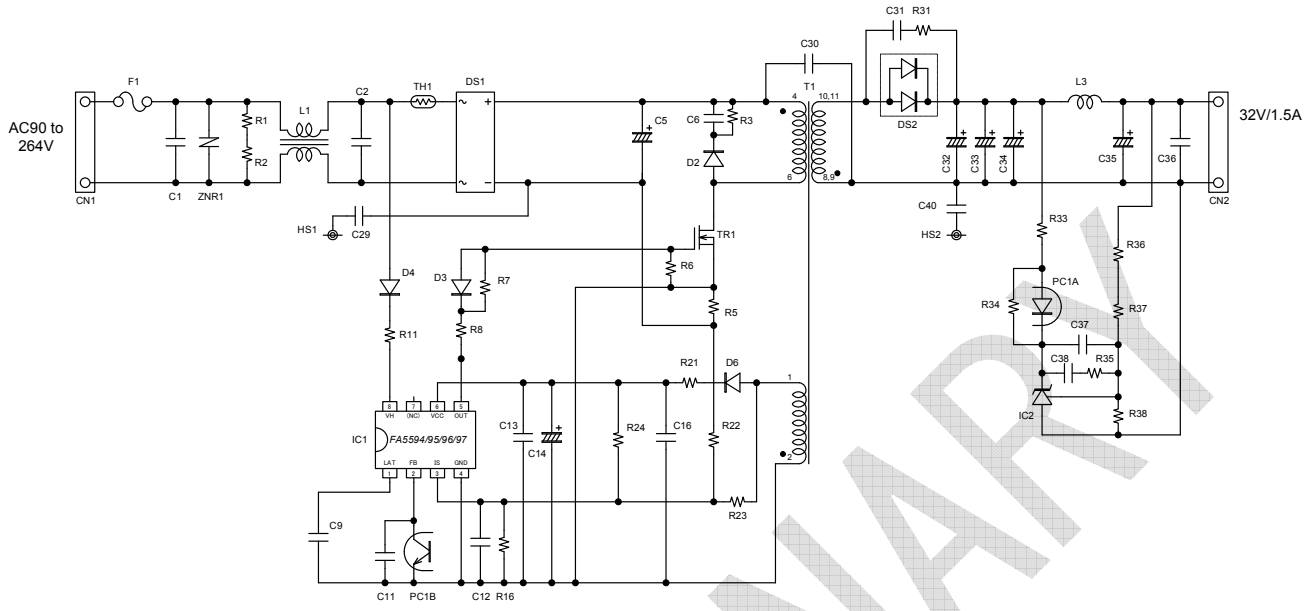
Example:
When the VH terminal is connected to a half-wave rectifier circuit with 100VAC input, the average voltage to be applied to the VH terminal is calculated to be approximately 45V, and the average current to be fed to the VH terminal is approximately 130μA;.
Furthermore, assuming that Tj = 25°C, VCC = 18V, and Qg = 80nC, and based on

IHrun=100uA (typ.)
ICCop1=1.4mA (typ.)
fsw=65kHz (typ.)

the loss of the IC having standard characteristics can be calculated as follows:

$$Pd \fallingdotseq 18V \times (1.4mA + 80nC \times 65kHz) + 45V \times 100uA \fallingdotseq 123\ mW$$

１０．Application circuit example



Note)

This application circuit example shows typical directions for use of this IC for reference and does not guarantee the operation and characteristics.

▪ Be sure to connect C13 (0.1 uF to 1 uF) to the VCC terminal in order to eliminate high-frequency noise.

▪ If light-load correction resistor R24 is applied between the OUT terminal and the IS terminal, you need not connect C16 (0.1 uF to 1uF).

▪ Resistor R16 (minus correction resistor of the IS terminal threshold voltage) between the IS terminal and the GND termina shall be several 10kΩ to OPEN.