FUJI Power Supply Control IC

FA7729R

Application Note

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Fuji Electric Device Technology Co., Ltd.
Power Supply Application Division

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- Personal equipment • Industrial robots etc.

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- Space equipment • Aeronautic equipment • Atomic control equipment
- Submarine repeater equipment • Medical equipment

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CONTENTS

Note

• Parts tolerance and characteristics are not defined in all application described in this Data book. When design an actual circuit for a product, you must determine parts tolerances and characteristics for safe and stable operation.

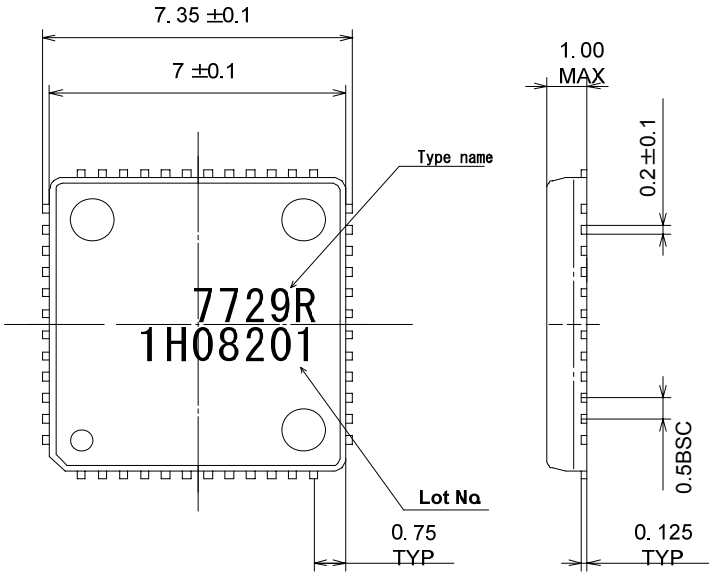
1. Description

FA7729R is a PWM type DC-to-DC converter control IC with 6channel outputs that can directly drive power MOSFETs. CMOS devices with high breakdown voltage are used in this IC and low power consumption is achieved. Furthermore, this IC can operate with wide range supply voltage from 2.5V to 18V
This IC is suitable for very small DC-to-DC converters because of 48pin VQFN mold package.

2. Features

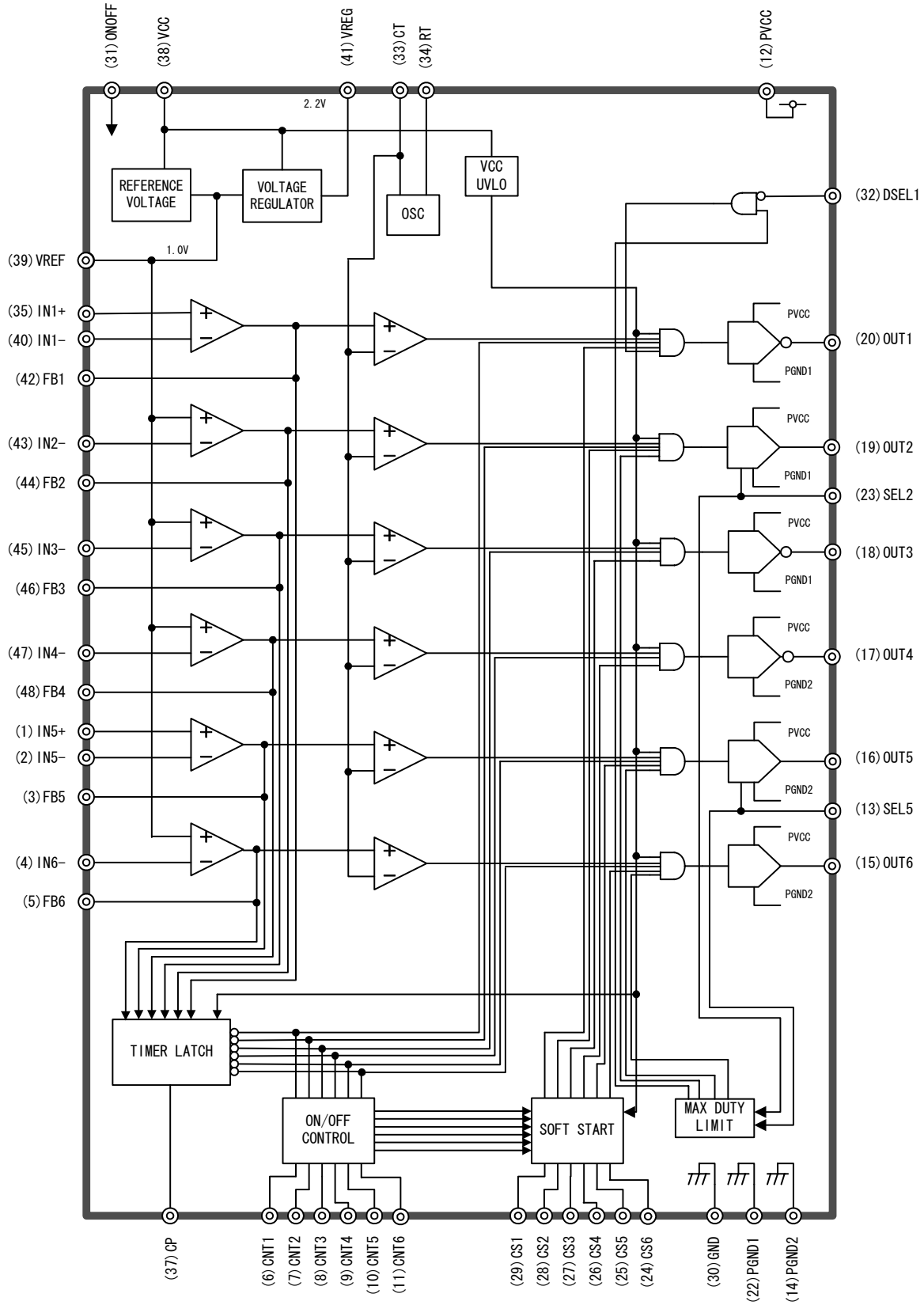
- MOSFET direct driving
- Low operating current by CMOS process: 3.3mA(typ.)
- 6channel PWM control IC
- High frequency operation: 50kHz to 800kHz
- Soft start function on each channel
- ON/OFF control on each channel
- Selectable output stage for P-channel / N-channel MOSFET on OUT2 and OUT5
- Maximum output duty cycle: 85% (typ.), except P-channel drive stage of OUT2(100%),OUT5 (100%) and mode selected by DEL1 pin of OUT1(100%).
- Built-in under voltage lockout
- High accuracy reference voltage: V_{REF}: 1.00V ±1%, V_{REG}: 2.2V ±2.3%
- Timer latch for short-circuit protection
- Thin and small package: VQFN-48

3. Outline



Unit: mm

4. Block diagram



5. Pin assignment

Pin No.	Pin symbol	Description	Pin No.	Pin symbol	Description
1	IN5+	CH.5 non-inverting input of error amplifier	25	CS5	Soft start for CH.5
2	IN5-	CH.5 inverting input of error amplifier	26	CS4	Soft start for CH.4
3	FB5	CH.5 output of error amplifier	27	CS3	Soft start for CH.3
4	IN6-	CH.6 inverting input of error amplifier	28	CS2	Soft start for CH.2
5	FB6	CH.6 output of error amplifier	29	CS1	Soft start for CH.1
6	CNT1	CH.1 control	30	GND	Ground
7	CNT2	CH.2 control	31	ONOFF	On/Off control
8	CNT3	CH.3 control	32	DSEL1	CH.1 selection of maximum duty limit
9	CNT4	CH.4 control	33	CT	Timing capacitor for oscillator
10	CNT5	CH.5 control	34	RT	Timing resistor for oscillator
11	CNT6	CH.6 control	35	IN1+	CH.1 non-inverting input of error amplifier
12	PVCC	Power supply for driver	36	(NC)	
13	SEL5	CH.5 selection of type of driven MOSFET	37	CP	Timer latched short circuit protection
14	PGND2	Ground for driver	38	VCC	Power supply (Over 2.5V)
15	OUT6	CH.6 series regulator driver output	39	VREF	Reference voltage
16	OUT5	CH.5 driver output	40	IN1-	CH.1 inverting input of error amplifier
17	OUT4	CH.4 driver output	41	VREG	Regulated voltage output
18	OUT3	CH.3 driver output	42	FB1	CH.1 output of error amplifier
19	OUT2	CH.2 driver output	43	IN2-	CH.2 inverting input of error amplifier
20	OUT1	CH.1 driver output	44	FB2	CH.2 output of error amplifier
21	(NC)		45	IN3-	CH.3 inverting input of error amplifier
22	PGND1	Ground for driver	46	FB3	CH.3 output of error amplifier
23	SEL2	CH.2 selection of type of driven MOSFET	47	IN4-	CH.4 inverting input of error amplifier
24	CS6	Soft start for CH.6	48	FB4	CH.4 output of error amplifier

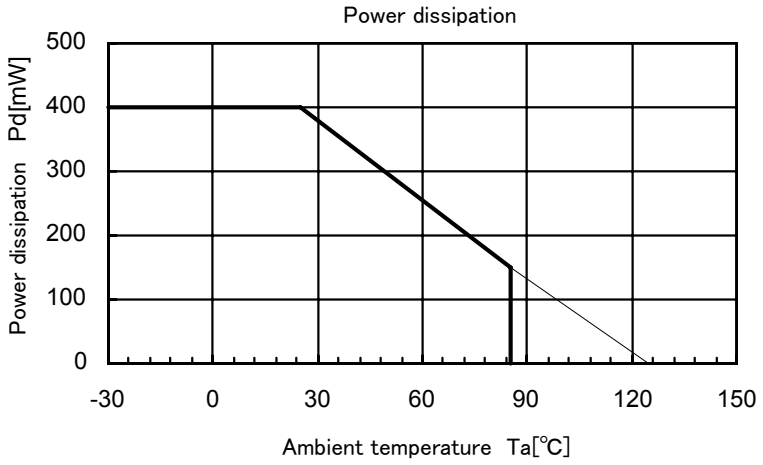
6. Ratings and characteristics

Following data are subject to change without notice. When using this IC, be sure to obtain the latest specifications.

(1) Absolute maximum ratings

Item	Symbol	Test condition	Rating	Unit
Power supply voltage (VCC)	V_{CC}		20	V
Power supply voltage (PVCC1)	V_{PCC}		20	V
ONOFF pin voltage	V_{ONOFF}		-0.3 to 5.0	V
DSEL1, SEL2, SEL5 pin voltage	V_{SEL}		-0.3 to 5.0	V
Input pin voltage of error amplifier (IN1+,IN1-,IN2+,IN2-,IN3-,IN4- IN5+,IN5-,IN6-)	V_{AMP_IN}		-0.3 to 5.0	V
Output pin voltage of error amplifier (FB1,FB2,FB3,FB4,FB5,FB6)	V_{AMP_OUT}		-0.3 to 2.5	V
CNT pin voltage（CNT1,2,3,4,5,6）	V_{CNT}		-0.3 to 5.0	V
Soft start pin voltage（CS1,2,3,4,5）	V_{CS}		-0.3 to 2.5	V
CP,CT,RT,VREG,VREF pin voltage	V_{CTR_IN}		-0.3 to 2.5	V
OUT1/2/3/4/5/6 source current (peak)	I_{OUT-}		-200	mA
sink current (peak)	I_{OUT+}		100	mA
OUT1/2/3/4/5 /6source current (continuous)	I_{OUT-}		-40	mA
sink current (continuous)	I_{OUT+}		40	mA
Power dissipation □1	P_d	Ta□25□	400	mW
Operating junction temperature	T_J		+125	deg
Operating ambient temperature	T_{OPR}		-30 to +85	deg
Storage temperature	T_{STG}		-40 to +125	deg

※1：Derating factor Ta<25deg : 4mW/deg



(2) Recommended operating conditions

Item	Symbol	Test condition	MIN	TYP	MAX	Unit
Power supply voltage (VCC)	V_{CC}		2.5	-	18	V
Power supply voltage (PVCC)	V_{PCC}		-	V_{CC}	-	V
ONOFF pin voltage	V_{ONOFF}		0.0	-	4.0	V
DSEL1,SEL2,SEL5 pin voltage	V_{SEL}		0.0	-	V_{REG}	V
Input pin voltage of error amplifier	V_{AMP_IN}		0.0	-	4.0	V
Output pin voltage of error amplifier	V_{AMP_OUT}		0.0	-	V_{REG}	V
CNT pin voltage	V_{CNT}		0.0	-	4.0	V
Soft start pin voltage	V_{CS}		0.0	-	2.5	V
Oscillation frequency	f_{OSC}		50	-	800	kHz
VREG pin capacitance	C_{REG}			1.0		µF
VREF pin capacitance	C_{REF}			0.1		µF

(3) Electrical characteristics

* The characteristics are based on the condition of V_{CC}=3.3V, Ta=+25deg, R_T=10kΩ, C_T=470pF, C_{REG}=1.0µF, C_{REF}=0.1µF, unless otherwise specified.

(1) Under voltage lockout circuit section (VCC pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
ON threshold voltage of VCC	V_{THUV}		2.05	2.20	2.35	V
Hysteresis voltage	V_{HYSUV}			0.1		V

(2) Reference voltage section (VREF pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Reference voltage	V_{REF}	C_{REF}=1µF, No load	0.99	1.00	1.01	V
Line regulation	V_{REF_LINE}	V_{CC}=2.5 to 12V		±3	±7	mV
Variation with temperature	V_{REF_TC}	Ta= -30 to 85deg		±0.5		%
Load regulation	V_{REF_LOAD}	I_{REF}=0 to 30µA	-15	-7		mV

(3) Regulated voltage for internal control blocks (VREG pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Regulated voltage	V_{REG}	C_{REG}=1µF, No load	2.15	2.20	2.25	V
Line regulation	V_{REG_LOAD}	V_{CC}=2.5 to 12V		±6	±15	mV
Variation with temperature	V_{REG_TC}	Ta= -30 to 85deg		±0.5		%
Load regulation	V_{REG_LOAD}	I_{REG}=0 to 5mA	-5	-2		mV

(4) Oscillator section (CT･RT pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Oscillation frequency	f_{OSC}	R_T=10kΩ,C_T=470pF	180	200	220	kHz
		R_T=10kΩ,C_T=150pF		550		kHz
Line regulation	f_{OSC_LINE}	V_{CC}=2.5 to 12V		±2	±8	%
Oscillation amplitude	V_{OSC_HI}	R_T=10kΩ,C_T=470pF		1.35		V
	V_{OSC_LO}			0.82		V
Variation with temperature	f_{OSC_TC}	Ta= -30 to 85deg		±3		%

(5) Error Amplifier section (IN1+,IN1-,FB1,IN2-,FB2,IN3-,FB3,IN4-,FB4,IN5+,IN5-,FB5,IN6-,FB6 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input offset voltage	V_{IO}				±10	mV
Common mode input voltage	V_{COM}		0.2		1.5	V
Open loop gain	A_{VO}			75		dB
Unity gain bandwidth	f_T			1.5		MHz
Output sink current	I_{SI}	$V_{IN-}=V_{FB}$, $V_{FB}=V_{REF}+50mV$	3.7	6.0	8.3	mA
Output source current	I_{SO}	$V_{IN-}=V_{FB}$, $V_{FB}=V_{REF}-50mV$	-200	-140	-90	µA

(6) Soft start section (CS1,CS2,CS3,CS4,CS5 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
CS pin source current	I_{CS}		-2.5	-2.0	-1.5	µA
Variation with temperature	I_{CS_TC}	Ta= -30 to 85deg		±12		%
Threshold voltage	V_{CSD10}	Duty cycle =10%		0.88		V
	V_{CSD80}	Duty cycle =80%		1.25		V

(7) Maximum duty limit section (DSEL1,SEL2,SEL5 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Maximum duty limit	D_{MAX}	OUT1 (DSEL1=VREG)	-	100	-	%
		OUT1 (DSEL1=GND)	80	85	90	%
		OUT2 (SEL2=VREG)	-	100	-	%
		OUT2 (SEL2=GND)	80	85	90	%
		OUT3, OUT4	-	100	-	%
		OUT5 (SEL5=VREG)	-	100	-	%
		OUT5 (SEL5=GND)	80	85	90	%
		OUT6	80	85	90	%

(8) CH.1 Maximum duty limit select section (DSEL1 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Duty limit enable	V_{DSEL_ON}		0		0.2	V
Duty limit disable	V_{DSEL_OFF}		V_{REG}-0.2		V_{REG}	V

(9) Timer latch protection section (CP pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Charge current of CP	I_{CP}		-2.5	-2.0	-1.5	μA
CP pin threshold voltage	V_{THCP}		1.6	1.75	1.9	V
FB pin threshold voltage	V_{THFB}		1.45	1.65	1.85	V

(10) On/Off control (ONOFF pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Threshold voltage	$V_{THONOFF}$	High state: on, Low state: off	0.35		0.85	V

(11) Channel control (CNT1, CNT2, CNT3, CNT4, CNT5, CNT6 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Threshold voltage	V_{THCNT}	High state: on, Low state: off	0.8		1.6	V

(12) Output section (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
High side on resistance	R_{ONHI}	I_{OUT}=-10mA		15	23	Ω
Low side on resistance	R_{ONLO}	I_{OUT}=10mA		7	11	Ω

(13) Selection of type of driven MOSFET section (SEL2, SEL5 pin)						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Voltage for driving Nch-MOSFET	V_{SEL_N}		0		0.2	V
Voltage for driving Pch-MOSFET	V_{SEL_P}		V_{REG}-0.2		V_{REG}	V

(14) Overall section						
Item	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Standby current	I_{CC0}	OFF mode by ONOFF pin		3	10	μA
Operating mode supply current	I_{CCA}	Operating mode		3.3		mA

(4) Output control logic table

a) ONOFF / CNT pin vs. Soft start pin state (CS)

	CNT pin						Soft start pin					
ONOFF	CNT1	CNT2	CNT3	CNT4	CNT5	CNT6	CS1	CS2	CS3	CS4	CS5	CS6
L	*	*	*	*	*	*	L	L	L	L	L	L
H	L	*	*	*	*	*	L	-	-	-	-	-
H	H	*	*	*	*	*	Charge	-	-	-	-	-
H	*	L	*	*	*	*	-	L	-	-	-	-
H	*	H	*	*	*	*	-	Charge	-	-	-	-
H	*	*	L	*	*	*	-	-	L	-	-	-
H	*	*	H	*	*	*	-	-	Charge	-	-	-
H	*	*	*	L	*	*	-	-	-	L	-	-
H	*	*	*	H	*	*	-	-	-	Charge	-	-
H	*	*	*	*	L	*	-	-	-	-	L	-
H	*	*	*	*	H	*	-	-	-	-	Charge	-
H	*	*	*	*	*	L	-	-	-	-	-	L
H	*	*	*	*	*	H	-	-	-	-	-	Charge

※ H：High state, L：Low state, *：Optional, -：Cannot control by the ONOFF/CNT pin

b) ONOFF / CNT pin vs. OUT pin state

	CNT pin						OUT pin					
ONOFF	CNT1	CNT2	CNT3	CNT4	CNT5	CNT6	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6
L	*	*	*	*	*	*	OFF	OFF	OFF	OFF	OFF	OFF
H	L	*	*	*	*	*	OFF	-	-	-	-	-
H	H	*	*	*	*	*	SW	-	-	-	-	-
H	*	L	*	*	*	*	-	OFF	-	-	-	-
H	*	H	*	*	*	*	-	SW	-	-	-	-
H	*	*	L	*	*	*	-	-	OFF	-	-	-
H	*	*	H	*	*	*	-	-	SW	-	-	-
H	*	*	*	L	*	*	-	-	-	OFF	-	-
H	*	*	*	H	*	*	-	-	-	SW	-	-
H	*	*	*	*	L	*	-	-	-	-	OFF	-
H	*	*	*	*	H	*	-	-	-	-	SW	-
H	*	*	*	*	*	L	-	-	-	-	-	OFF
H	*	*	*	*	*	H	-	-	-	-	-	ON

※ H：High state, L：Low state, *：Optional

※ OFF：Off mode, SW：Switching mode, -：Cannot control by the ONOFF/CNT pin

※ In case of CNT pin set to low state, OUT pins switching is stopped by the discharge of CS pin. Therefore when CNT pin changes from high state to low state, OUT pins switching is continued until CS pin has discharged.

c) ONOFF / CNT pin vs. Time latch detect function

	CNT pin						OUT pin					
ONOFF	CNT1	CNT2	CNT3	CNT4	CNT5	CNT6	CH.1	CH.2	CH.3	CH.4	CH.5	CH.6
L	*	*	*	*	*	*	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
H	L	*	*	*	*	*	Invalid	-	-	-	-	-
H	H	*	*	*	*	*	Valid	-	-	-	-	-
H	*	L	*	*	*	*	-	Invalid	-	-	-	-
H	*	H	*	*	*	*	-	Valid	-	-	-	-
H	*	*	L	*	*	*	-	-	Invalid	-	-	-
H	*	*	H	*	*	*	-	-	Valid	-	-	-
H	*	*	*	L	*	*	-	-	-	Invalid	-	-
H	*	*	*	H	*	*	-	-	-	Valid	-	-
H	*	*	*	*	L	*	-	-	-	-	Invalid	-
H	*	*	*	*	H	*	-	-	-	-	Valid	-
H	*	*	*	*	*	L	-	-	-	-	-	Invalid
H	*	*	*	*	*	H	-	-	-	-	-	Valid

※ H：High state, L：Low state, *：Optional, -：Cannot control by the ONOFF/CNT pin.

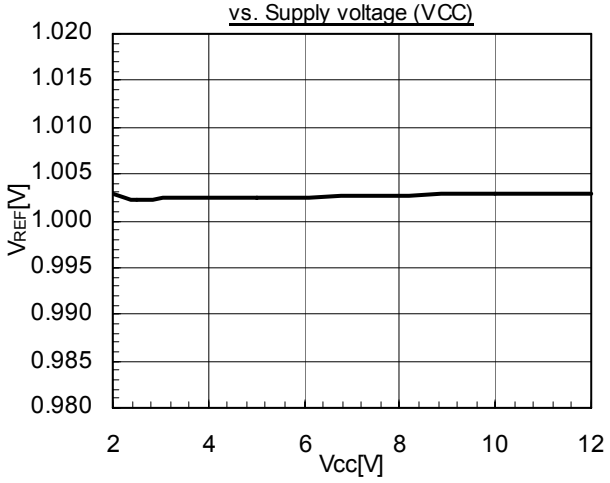
d) Selection of type of driven MOSFET

Select pin			OUT state			Maximum duty limit		
DSEL1	SEL2	SEL5	OUT1	OUT2	OUT5	DMAX1	DMAX2	DMAX5
L	*	*	- (P)	-	-	Valid	-	-
H	*	*	- (P)	-	-	Invalid	-	-
*	L	*	-	N	-	-	Valid	-
*	H	*	-	P	-	-	Invalid	-
*	*	L	-	-	N	-	-	Valid
*	*	H	-	-	P	-	-	Invalid

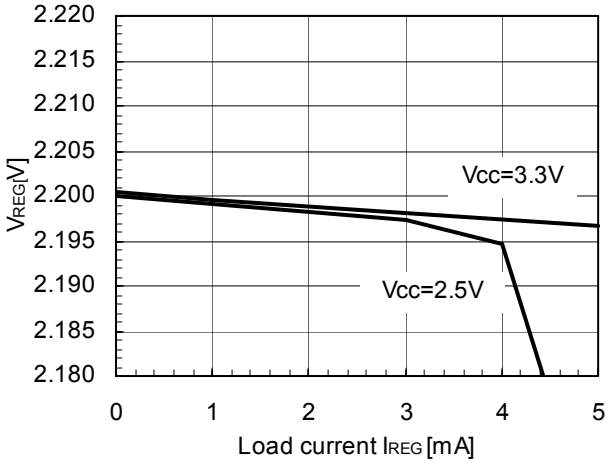
※ H：High state, L：Low state, *：Optional, -：Cannot control by the ONOFF/CNT pin.
※ N：You can drive N-channel MOSFET or NPN bipolar transistor.
※ P：You can drive P-channel MOSFET or PNP bipolar transistor.

7. Characteristic curves

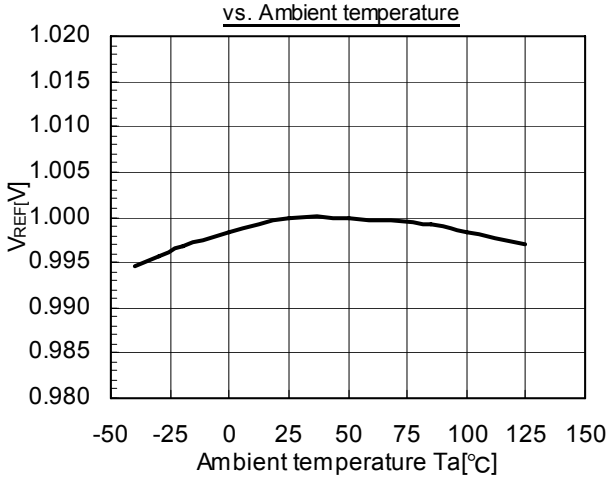
Reference voltage (VREF)
vs. Supply voltage (VCC)



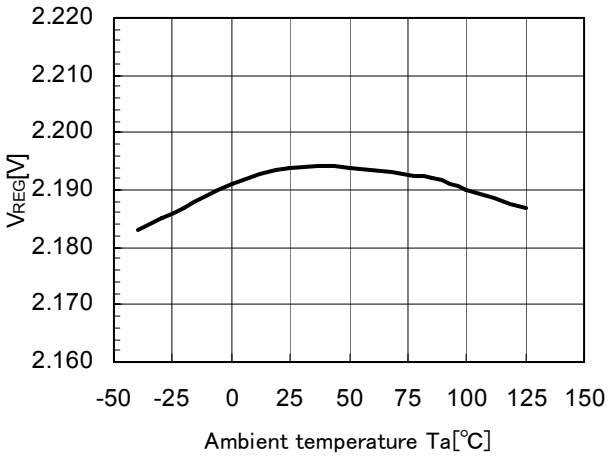
Regulated voltage(VREG) vs. Load current



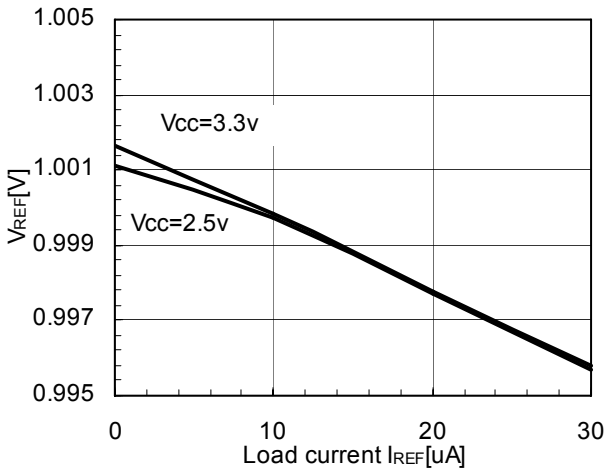
Reference voltage(VREF)
vs. Ambient temperature



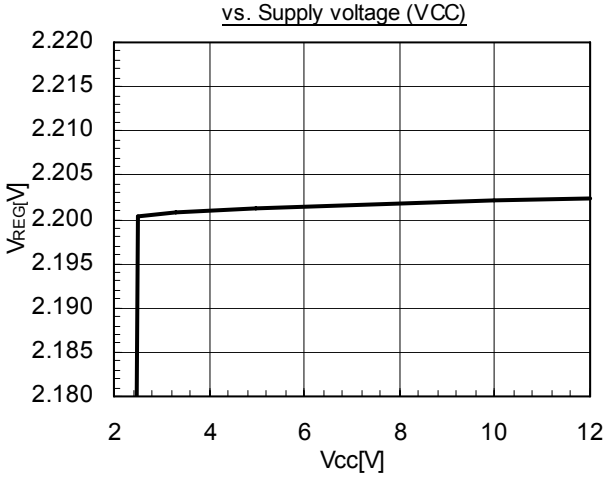
Regulated voltage (VREG)
vs. Ambient temperature



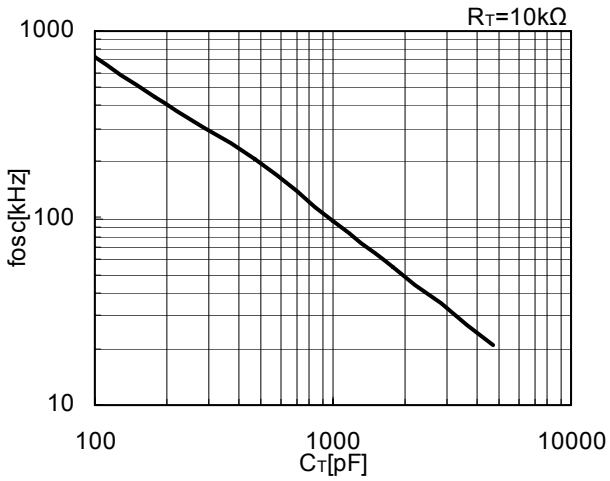
Reference voltage(VREF) vs. Load current



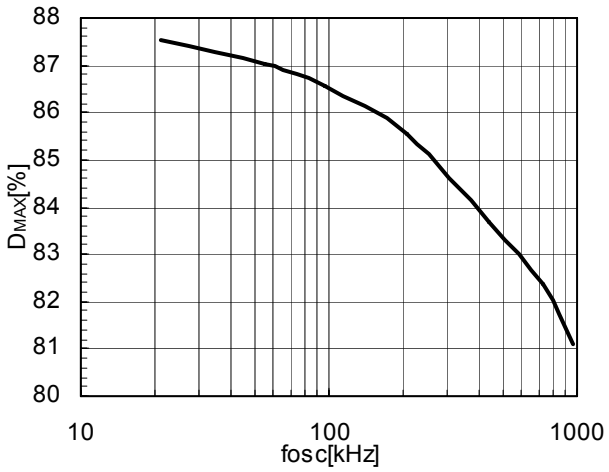
Regulated voltage (VREG)
vs. Supply voltage (VCC)



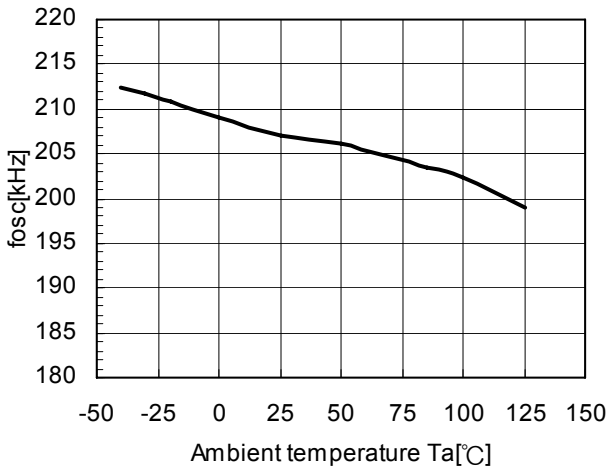
Timing capacitor CT vs. Oscillation frequency



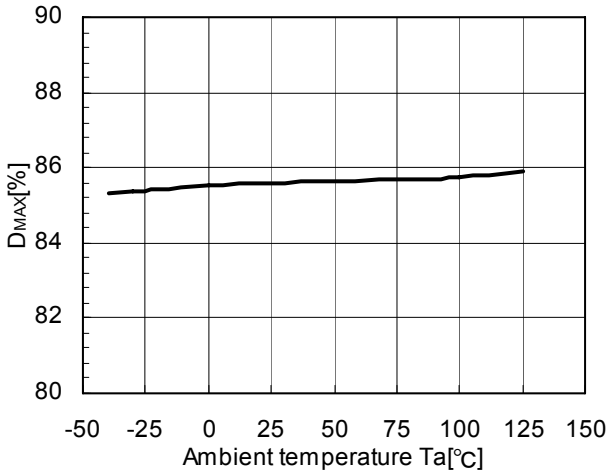
Maximum duty limit vs. Frequency



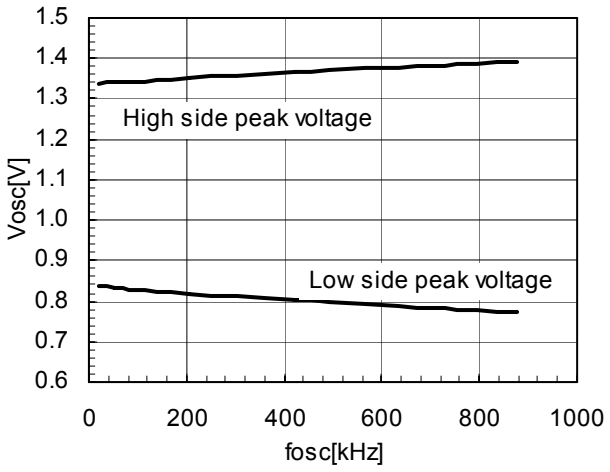
Oscillation frequency vs. Ambient temperature



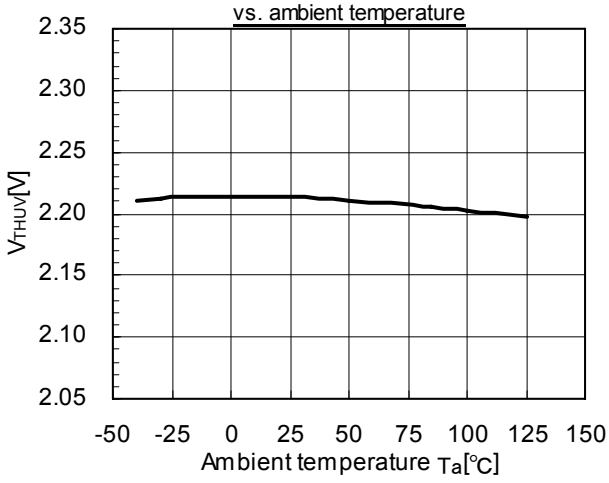
Maximum duty limit vs. Ambient temperature



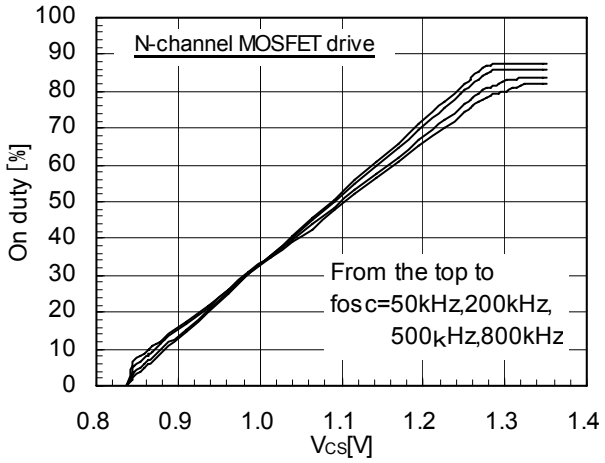
Oscillation amplitude vs. Oscillation frequency



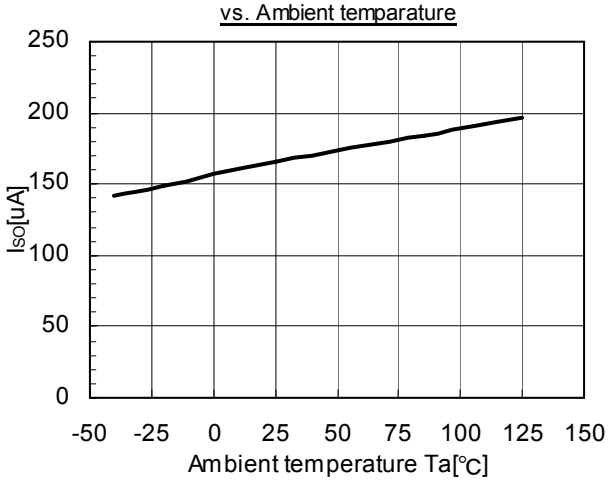
UVLO on threshold voltage vs. ambient temperature



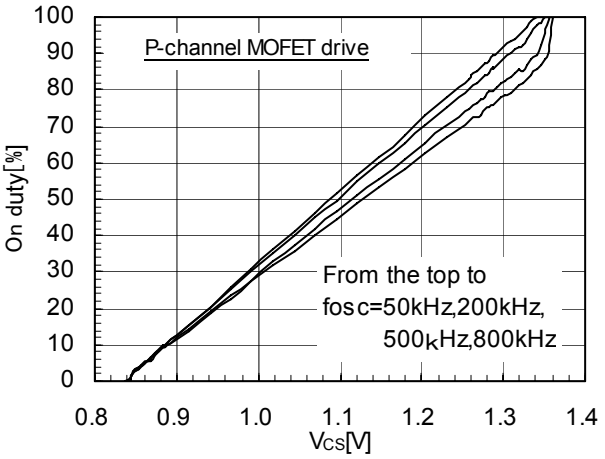
CS pin voltage vs. On duty



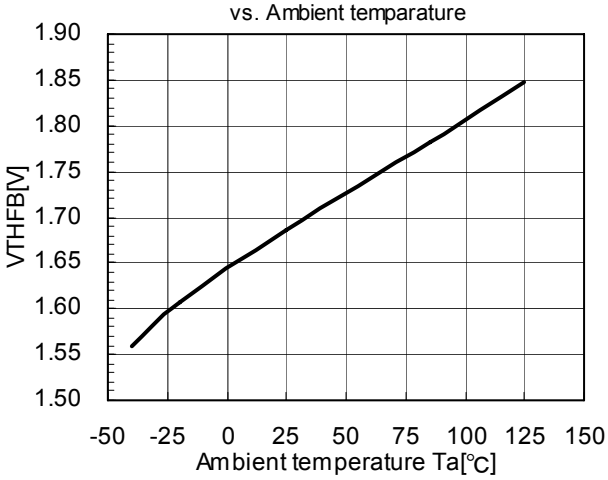
Output source current of error amplifier
vs. Ambient temparature



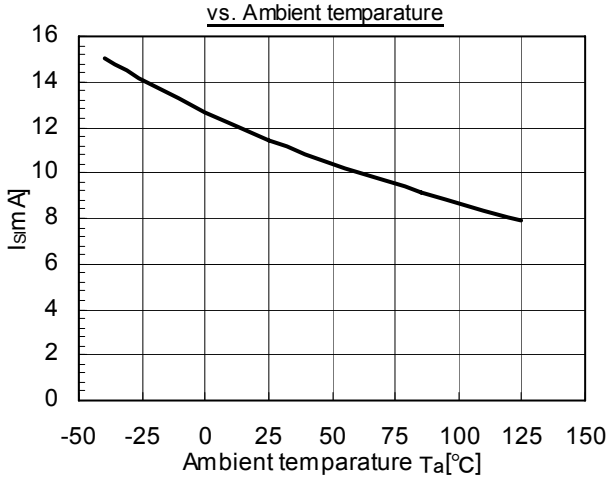
CS pin voltage vs. On duty



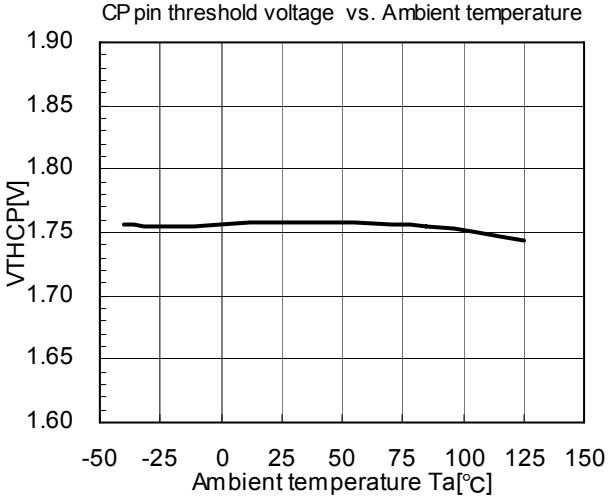
Timer latch threshold voltage of FB pin
vs. Ambient temparature



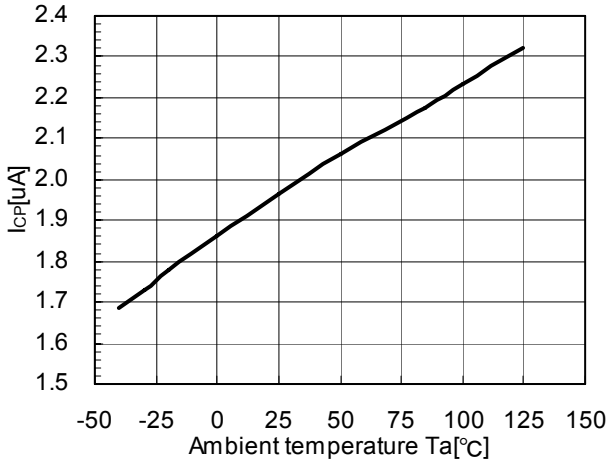
Output sink current of error amplifier
vs. Ambient temparature



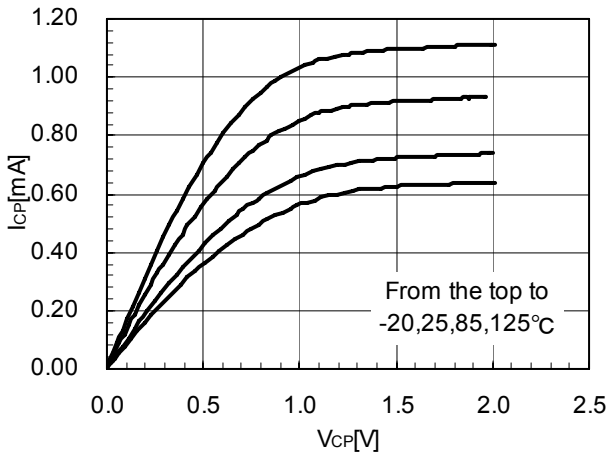
CP pin threshold voltage vs. Ambient temperature



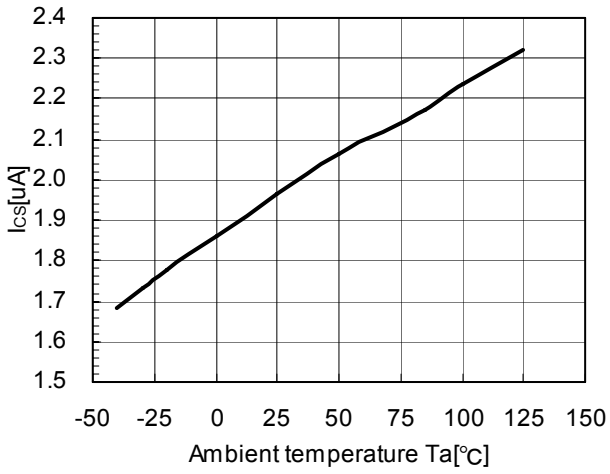
CP pin source current vs. Ambient temperature



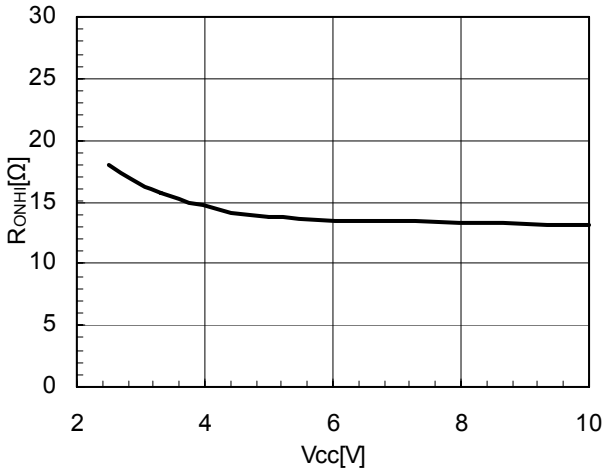
CP pin discharge switch current vs. voltage



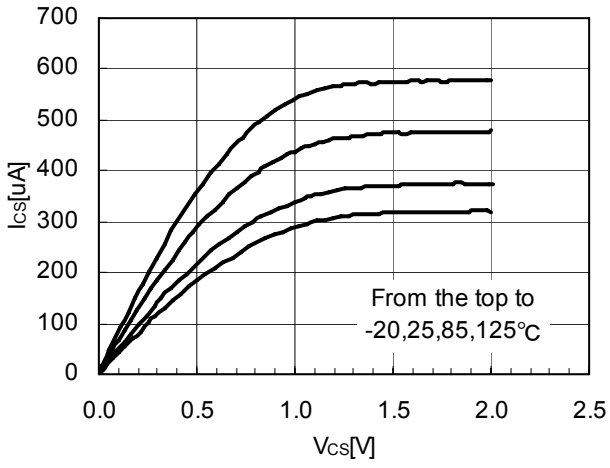
CS pin source current vs. Ambient temparature



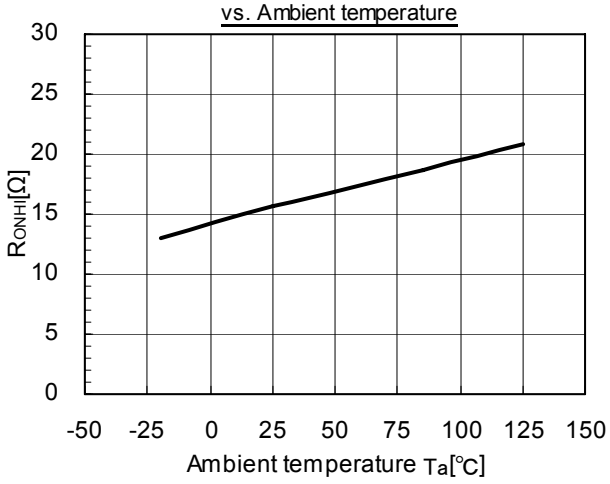
OUT pin high level on resitance vs. Supply voltage



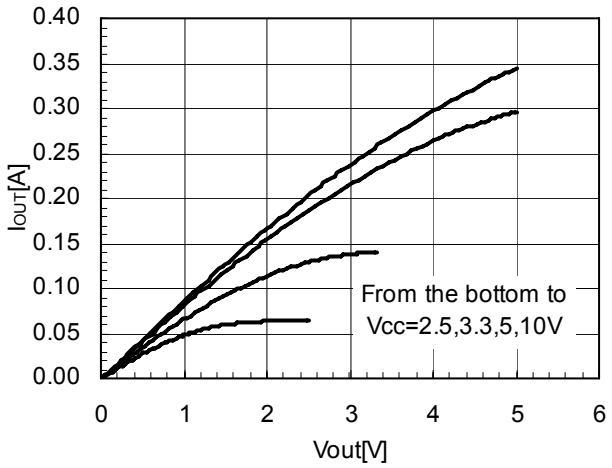
CS pin discharge switch current vs. voltage



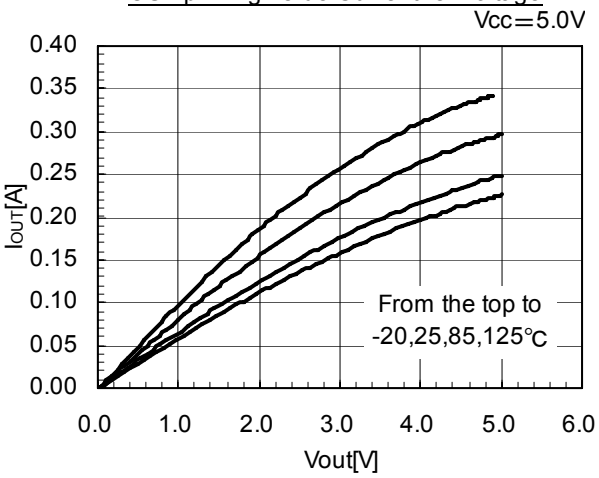
OUT pin high level on resistance vs. Ambient temperature



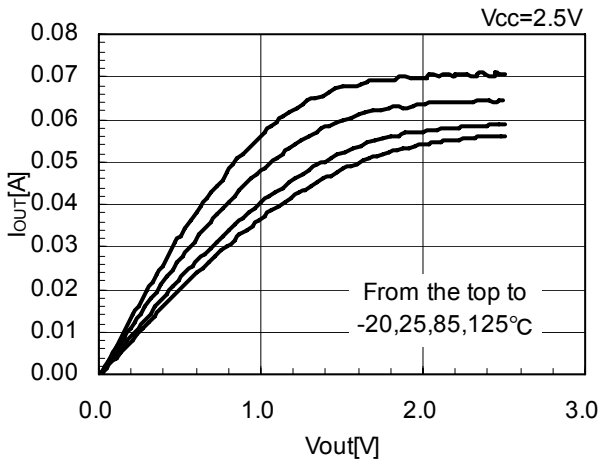
OUT pin High side Current vs. Voltage



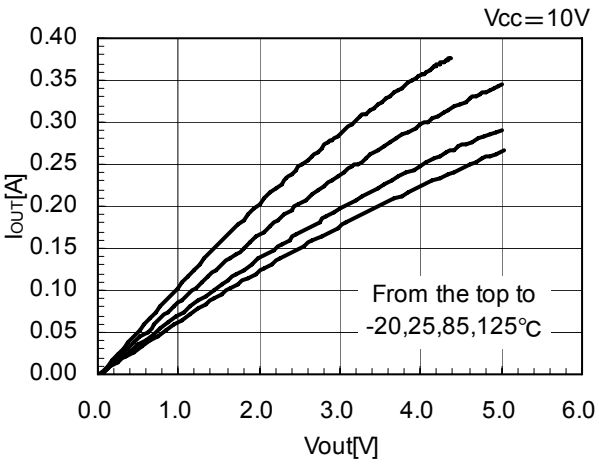
OUT pin High side Current vs. Voltage



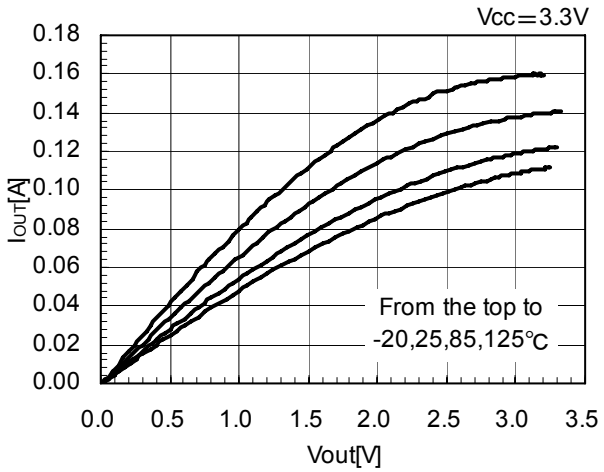
OUT pin High side Current vs. Voltage



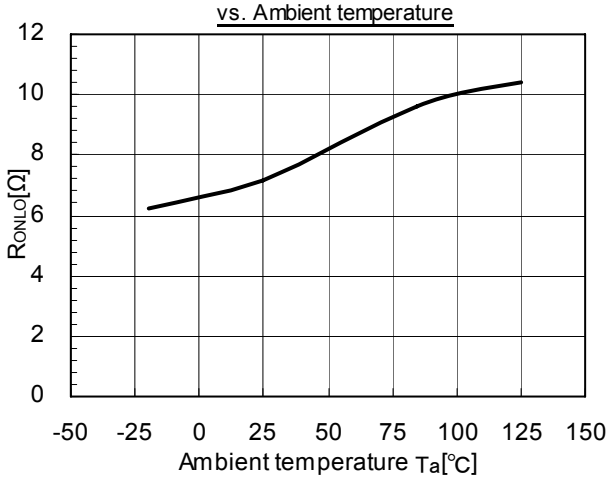
OUT pin High side Current vs. Voltage



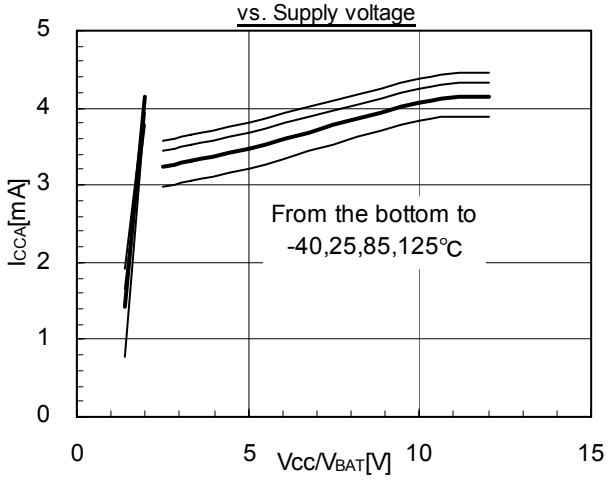
OUT pin High side Current vs. Voltage



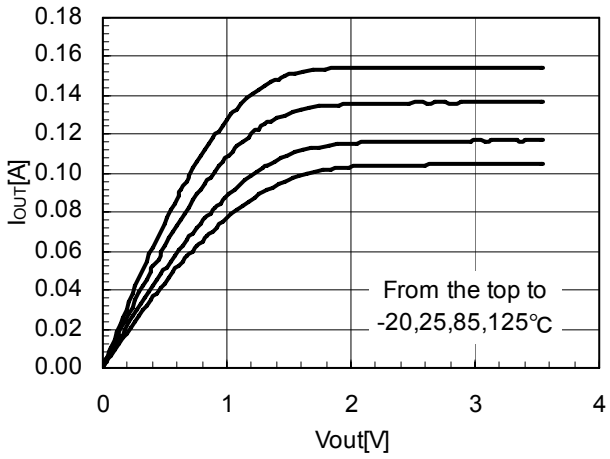
OUT pin low level on resistance vs. Ambient temperature



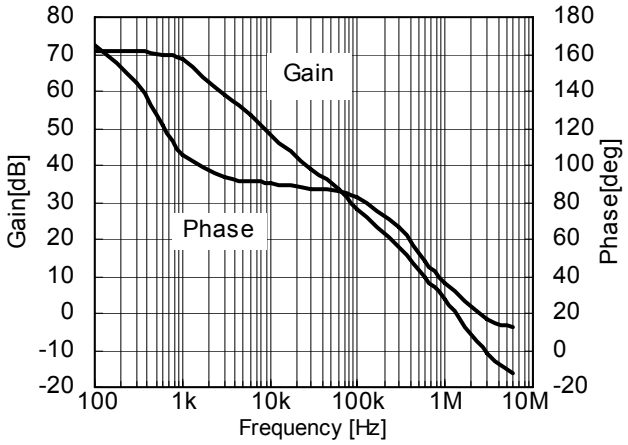
Operating mode supply current vs. Supply voltage



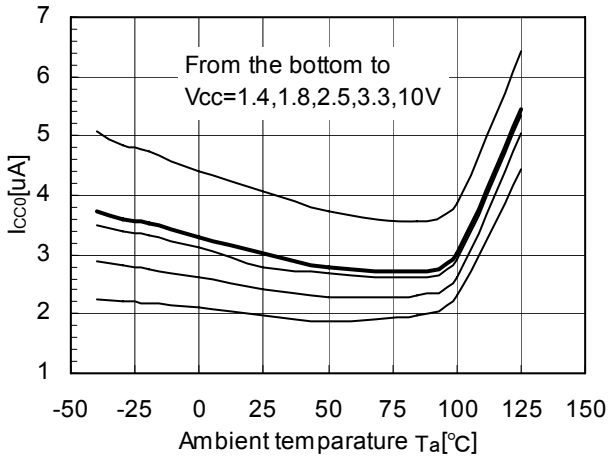
OUT pin Low side Current vs. Voltage



Error ampilifier gain and phase vs. frequency



Stand-by current vs. Ambient temparature



8. Description of each circuit

(1) Reference voltage circuit

This circuit generates the reference voltage (V_{REF}) of 1.00V±1% and the regulated voltage (V_{REG}) of 2.2V±2.3% compensated in temperature from VCC voltage. Both V_{REF} and V_{REG} are stabilized above 2.4V input of supply voltage (V_{CC}).

The reference voltage (V_{REF}) is connected to the non-inverting input of error amplifiers except amplifier 5. The V_{REF} voltage can be used as a regulated power supply by the VREF pin. In this case, the output current should be within 30μA.

The regulated voltage (V_{REG}) is provided as a regulated power supply. The output current circuit should be within 5mA. (In case of V_{CC}<3.3V should be within 3mA) The V_{REG} voltage also is used as a regulated power supply for IC's internal blocks.

VREF pin and VREG pin have to connect capacitors C_{REF} and C_{REG} for each pin in order to stabilize voltages (To determine capacitance, refer to recommended operating conditions).

(2)Oscillator

The oscillator generates a triangular waveform by charging and discharging the capacitor.

Oscillation frequency can be set by the value of resistor connected to the RT pin and the capacitor connected to the CT pin. (Fig.1)

The voltage oscillates between approximately 0.82V and 1.35V in almost the same charging and discharging gradients (Fig. 2).

Oscillation output is connected to PWM comparators.

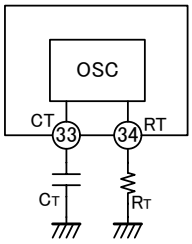


Fig.1

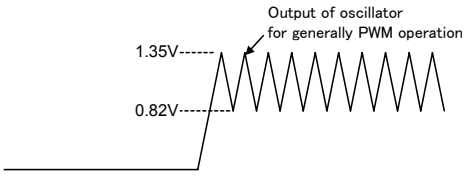


Fig.2

(3)Error amplifier

Error amplifiers have inverting input pins of IN*- pin. The non-Inverting inputs are internally connected to the reference voltage VREF (1.00V±1%; 25□), except error amplifier 5.

The error amplifier 5 has inverting input pin of IN5- pin (Pin2) and non-inverting input of IN5+ pin (Pin1). Since each input of error amplifier 5 is connected to the pins, the channel 5 is suitable for any circuit topology.

FB* pins are the output of the error amplifiers. An external RC network is connected between FB* pin and IN*- pin for gain and phase as compensation setting. (Fig.3)

The error amplifier 6 can be used for a series regulator.

For connecting of each topology, see Design Advice.

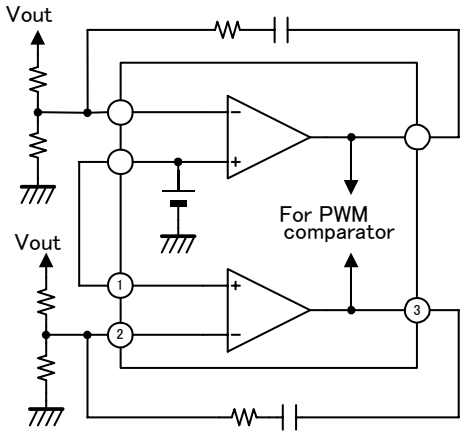


Fig.3

(4)PWM comparator

The PWM output is generated from the oscillator output, the error amplifier output (FB*) and CS voltage (CS*) (Fig. 4). The oscillator output is compared with the preferred lower voltage either FB* or CS*. While the preferred voltage is lower than oscillator output, the PWM output is low. While the preferred voltage is higher than oscillator output, the PWM output is high. (Cannot be observed externally)

The output polarity of OUT2, OUT5 changes according to the condition of SEL* pin. (See Fig. 6) N-channel drive output is set by connect SEL* pin to the GND, P-channel drive output is set by connect SEL pin to the VREG.

The maximum duty cycle is internally set to 85% (typ.). When OUT2 and OUT5 are set to P-channel operation mode (SEL*=VREG), the maximum duty cycle is not limited (100%).

The Internal maximum duty cycle of OUT1 is selected by DSEL1 pin. 100% at DSEL1=VREG and 85%(typ.) at DSEL1=GND for the use of Inverting circuit.

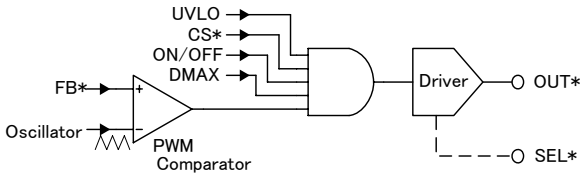


Fig.4

(5)Soft start circuit

The capacitor for soft start C_{CS*} is connected to the CS* pin. (Fig.5)

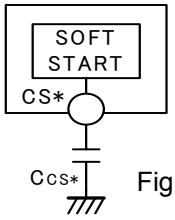


Fig.5

When the supply voltage is applied to the VCC pin and UVLO is cancelled, the capacitor C_{CS*} is charged by the internal constant current sources (2μA, typ.). Then, the CS* voltage gradually increases. Since the CS* pin are connected to the PWM comparator, the pulses gradually widen and then the soft start function operates. (Fig. 6)

Otherwise when you start up by the CNT* pin, soft start function operates in the same way.

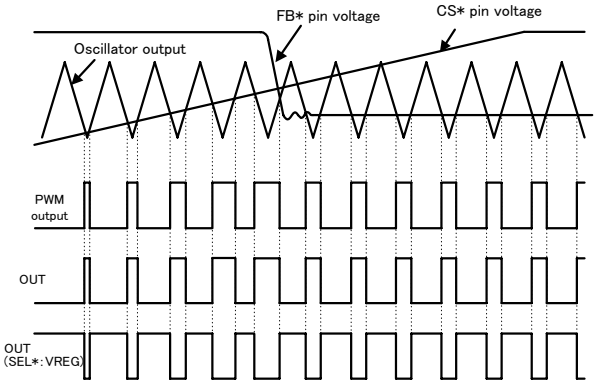


Fig.6

(6)Timer latch short-circuit protection

This IC has timer latch short-circuit protection . This function cuts off the output of all channels when the output voltage of DC-to-DC converter drops due to short circuit or overload. To set delay time for timer latch operation, a capacitor C_{CP} should be connected to the CP pin (Fig. 7).

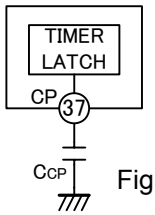


Fig.7

When one of the output voltage of the DC-to-DC converter drops due to short circuit or overload, the FB* pin voltage increases up to around the VREG voltage. When the FB* pin voltage exceeds 1.85V(max.), constant current source (2μA typ.) starts charging the capacitor C_{CP} connected to the CP pin. If converter drops do not cancel, charging the C_{CP} continues and reaches the condition of the CP pin voltage exceeds 1.9 V (max.), the circuit regards the case as abnormal. Then the IC is set to off latch mode and outputs of all channels are shut off (Fig. 8).

The period (tp) between the occurrence of short-circuit in the converter output and setting to off latch mode can be calculated by the following equation:

$$tp[\mathrm{s}] = C_{CP} \cdot \frac{V_{THCPTL}}{I_{CP}}$$

V_{THCPTL}: CP pin latched mode threshold voltage [V]
I_{CP}: CP charge source current [μA]
C_{CP}: Capacitance of CP pin capacitor

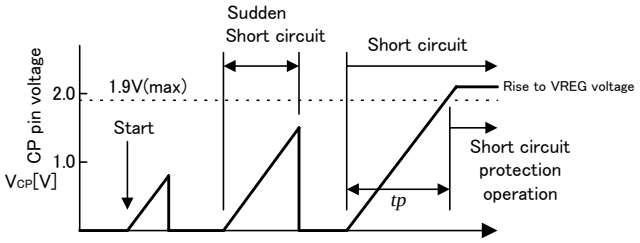


Fig.8

You can reset off latched mode of the short-circuit protection by either of the following ways about 1) CP pin, or 2) VCC pin, or 3) CNT* pin:

1) CP voltage = 0V
2) VCC voltage set to below the UVLO voltage (2.2V,typ.)
3) Set the CNT* pin of off latched mode caused channel to the GND (Off the channel)

If the timer-latched mode is not necessary, connect the CP pin to the GND.

(7)ON/OFF Control function

Each channel can be on/off controlled by the input of external signals to the CNT* pin.

If output is operated to on mode, apply the voltage above 0.8V (min.) to the CNT* pin, then OUT* pin provides the pulse. At this time, the CS* voltage gradually increases, the pulses gradually widen and then the soft start function operates.

If output is operated to off mode, apply the voltage below 0.8V (min.) to the CNT* pin, then the CS* voltage is discharged and the output stops switching.

In order to reduce stand-by current, all output can be stopped by the ON/OFF pin (Pin31) setting to the voltage below 0.9V(max.). Stand-by current is 4μA (typ.).

If the Start-up circuit is necessary, connect the CNT1 pin (Pin6) to VREG, but OUT1 cannot control.

Attention for Stand-by mode

If you stop the IC's operation by ON/OFF pin (switch to the Low) when CNT* pin keeps ON mode (High), there is a possibility of generate the wrong pulse output and it causes the chattering of the output voltage or destruction of the external MOSFET by the non controlled pulse.

The reason of this wrong operation is by the unstable internal state of IC which caused from the shut down the internal power supply VREG by ON/OFF pin.

The measure for this wrong operation is make a sequence at shutdown time: shut down the CNT* pin at first, and finally shut down the ON/OFF pin.

(8)Under voltage lockout circuit

This IC contains a under voltage lockout circuit (UVLO) to protect the circuit from the damage caused by malfunctions when the supply voltage drops. UVLO for the VCC pin voltage and the VBAT pin voltage are contained individually.

In case of the VCC pin, when the supply voltage rises from 0V, the IC starts to operate at VCC of 2.2V(typ.) and outputs generate pulses. If a drop of the supply voltage occurs, it stops output at VCC of 2.1V(typ.). When it occurs, the CS* pin is turned to low level as reset the pin.

(9)Output circuit

This IC contains push-pull output stages and can directly drive MOSFETs. The maximum peak current of the output stage OUT1, OUT2, OUT3, OUT4,OUT5 and OUT6 are the sink current of +100mA, and the source current of - 200mA. This IC can also drive NPN and PNP bipolar transistors. The maximum current of bipolar transistors is ± 40mA. OUT6 pin is for series regulator control. The maximum current of series regulator control is ± 30mA. You must design the output current considering the rating of power dissipation. (See Design Advice)

You can switch the types of external discrete MOSFETs by wiring of the SEL* pins (Pin 23, Pin 13). For driving N-channel MOS, connect the SEL pins to the GND. For driving P-channel MOS, connect the SEL pins to the VREG. You can design buck converter by driving P-channel MOS, and boost converter by driving N-channel MOS.
Connect them either to GND or to VREG surely.

9. Design Advice

(1) Setting the oscillation frequency

As described at Section 8-(2), "Description of each circuit," a desired oscillation frequency of generally operation can be determined by the value of the resistor connected to the RT pin and the value of the capacitor connected to the CT pin, a desired oscillation frequency of Start-up operation can be determined by the value of the capacitor connected to the CTST pin. When designing an oscillation frequency, you can set any frequency between 300kHz and 1.5MHz of generally operation, and between 50kHz and 300kHz of Start-up operation.

You can obtain the oscillation frequency of generally operation from the characteristic curve "Timing capacitor capacitance (C_T) vs. Oscillation frequency (fosc)" or the value can be approximately calculated by the following expression: (At R_T=10kΩ)

$$f_{OSC} \approx 47 \times 10^3 \times C_T^{-0.9}$$

$$C_T \approx \left(\frac{47 \times 10^3}{f_{OSC}} \right)^{1.1}$$

fosc: Oscillation frequency [kHz]
C_T: Timing capacitor [pF]

This expression, however, can be used as rough calculation, the obtained value is not guaranteed. The operation frequency varies due to the conditions such as tolerance of the characteristics of the ICs, influence of noises, or external discrete components. When determining the values, examine the effectiveness of the values in an actual circuit. The timing resistor R_T, capacitor C_T should be wired to the GND pin as shortly as possible because these pins are high impedance pins and are easy affected by noises.

(2) Determining soft start period

The period from the start of charging the CS* pin to widening n% of output duty cycle can be roughly calculated by the following expression:

$$ts*\,[s] = \frac{V_{CS*n} \times C_{CS*}}{I_{CS}}$$

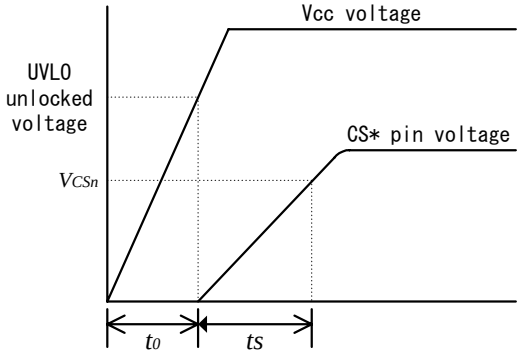
$V_{CS}*_n$: CS* pin voltage of n% of output duty cycle [V]
$C_{CS}*$: CS* pin timing capacitor [pF]
I_{CS}: CS* pin source current [μA] (2μA, typ.)

*VCS*n* is the voltage of the CS* pin in n% of output duty cycle, and vary in accordance with operating frequency. The value can be obtained from the characteristic curve "CS voltage vs. Output duty cycle".

If the capacitor connected to CS* pin has a leak current, the period of soft start will be change from desired value because CS* pin source current is so small.

The charging of the CS* pin starts after the UVLO is unlocked. Therefore, the period from power-on of VCC to widening n% of output duty cycle is the sum of t_0 and ts. (Fig.9)

To reset the soft start function, the supply voltage V_{CC} is lowered below the UVLO voltage (2.1V typ.) and then the internal switch discharges the CS* capacitor. Therefore, when determining the period of soft start in case of restarting the power supply, consider the characteristics carefully, else there is a possibility of invalid soft start.



t_0 : The period from power-on of VCC to UVLO unlocked

Fig.9

(3) Loss Calculation

Since it is difficult to measure IC loss directly, the calculation to obtain the approximate loss of the IC connected directly to a MOSFET is described below.

When the supply voltage is V_{CC}, the current consumption of the IC is I_{CC1}, the total input gate charge of the driven MOSFET is Qg, and the switching frequency is fsw, the total loss Pd of the IC can be calculated by:

$$Pd \approx Vcc \times (I_{CC1} + Qg \times fsw)$$

The value in this expression is influenced by the effects of the dependency of supply voltage, the characteristics of temperature, or the tolerance of parameter. Therefore, evaluate the appropriateness of IC loss sufficiently considering the range of values of above parameters under all conditions.

Example)

I_{CC1}=3.3mA for V_{CC}=6V in the case of a typical IC from the characteristics curve. Qg=6nC, fsw=200kHz, the IC loss "Pd" is as follows.

$$Pd \approx 6.0 \times (3.3mA + 6nC \times 200kHz) \approx 27mW$$

If five MOSFETs are driven under the same condition for 6 channels, Pd is as follows:

$$Pd \approx 6.0 \times \{3.3mA + 6 \times (6nC \times 200kHz)\}$$
$$\approx 63mW$$

(4) Pull up/down resistor at OUT* pins

The power supply for control blocks of OUT pin drivers is the V_{REG}. The V_{REG} voltage is not operated at the condition of IC's power supply V_{CC} below the UVLO voltage. Therefore, OUT* pins are unstable at V_{CC} below the UVLO voltage.

If you have this condition of V_{CC} and possibility of some trouble by unstable OUT* pins, connect pull up or pull down resistor to OUT* pins. (Fig.10)

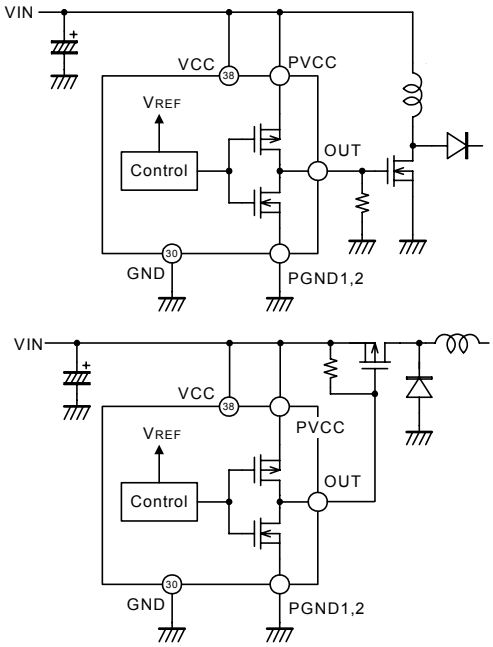


Fig.10

(5) Performance of output stage

The performance of output stages is the sink current (peak) of 100mA of and the source current (peak) of -200mA.

Switching speed is effected by external switching device, especially at high frequency, so examine the external switching device and frequency carefully.

If the performance of the ICs is not sufficient for your design, consider adding a buffer circuit to improve the performance.

.

(6) Attention for driving bipolar transistor

If you use bipolar transistor as a switching device, connect resistor R_B between Base of transistor and OUT* pin, else there is a possibility of destroy the IC by over current because OUT* pin driver does not contain a current limit resistor. (Fig.11) Output current of OUT* pins are below 40mA (continuous).

The connection of capacitor C_B is effective for speed up the switching.

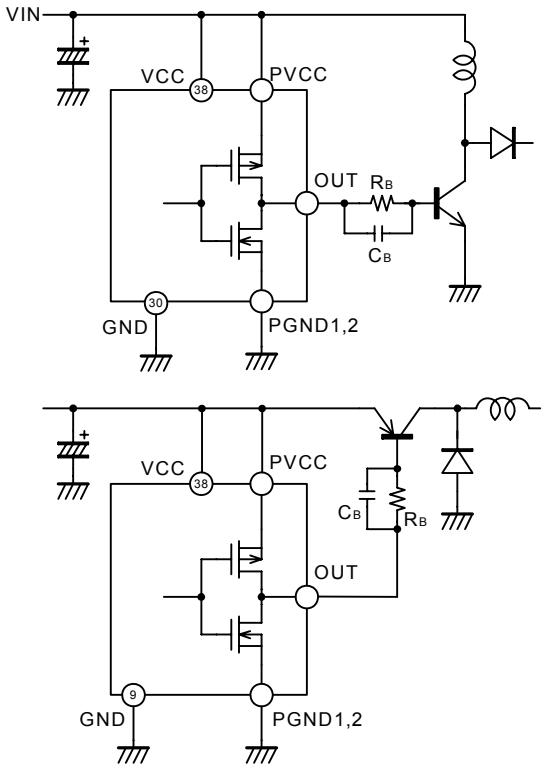


Fig.11

(7) Restriction of external discrete components and recommended operating conditions

To achieve a stable operation of the IC, the value of external discrete components and the voltage and the current applied to each pin should be within the recommended operating conditions.

If you have none use channel, connect its channel's CNT* pin to the GND.

P-channel MOSFETs are installed between the VCC pin and the OUT1 pin, and between the VCC pin and the OUT2 pin. Since the P-channel MOSFET has a parasitic diode, so if the voltage of OUT pins becomes higher than the VCC pin voltage, the current flows from each terminal to the VCC pin. Cautious care must be taken accordingly when designing.

(8) Determining the output voltage of DC-to-DC converters

Figure 12 to 17 shows the ways to the output voltage of DC-to-DC converter.

·Applications for each channels

CH1	Buck, Invert
CH2	Buck, Boost, Fly-back
CH3,4	Buck
CH5	Buck, Boost, Fly-back
CH6	Boost, Fly-back

The channel which can apply to Boost converter is also can apply to SEPIC type Buck/Boost converter. See Application Circuit.

In the case of a boost circuit in OUT1, the output voltage can be calculated as follows: (Fig.12)

$$Vout1 = \frac{R1 + R2}{R2} \times V_{REF}$$

In the case of a invert circuit in OUT1, the output voltage can be calculated as follows: (Fig.13)

$$Vout1 = \frac{R1 + R2}{R2} \times V1 - \frac{R1}{R2} \times V_{REG}$$

The ratio of resistance is as follows:

$$\frac{R2}{R1} = \frac{V_{REG} - V1}{V1 - V_{OUT1}}$$

$$V1 = \frac{R3}{R3 + R4} \times V_{REG}$$

In the case of a boost circuit in OUT2 and OUT6, the output voltage can be calculated as follows: (Fig.14)

$$Vout* = \frac{R5 + R6}{R6} \times V_{REF}$$

In the case of a buck circuit in OUT2, OUT3 and OUT4, the output voltage can be calculated as follows: (Fig.15)

$$Vout* = \frac{R7 + R8}{R8} \times V_{REF}$$

In the case of a buck circuit in OUT5, the output voltage can be calculated as follows: (Fig.16)

$$Vout5 = \frac{R9 + R10}{R10} \times V_{REF}$$

In the case of a boost circuit in OUT5, the output voltage can be calculated as follows: (Fig.17)

$$Vout5 = \frac{R11 + R12}{R12} \times V_{REF}$$

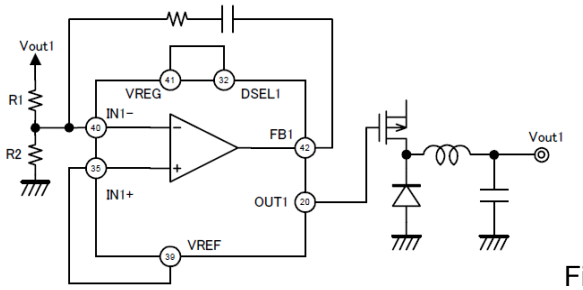


Fig.12

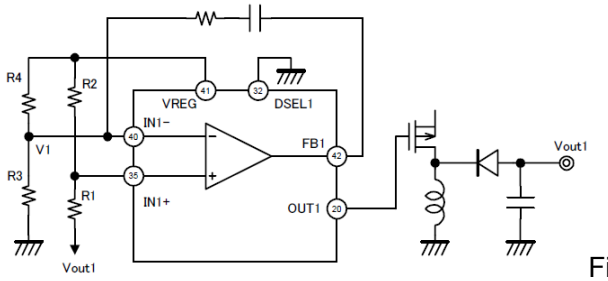


Fig.13

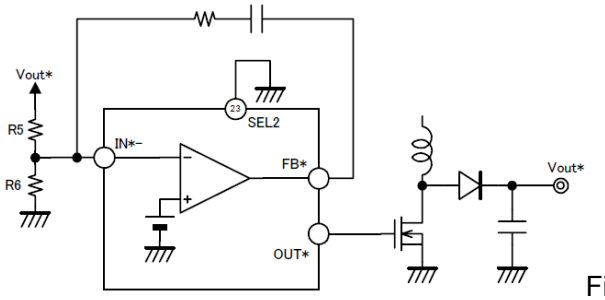


Fig.14

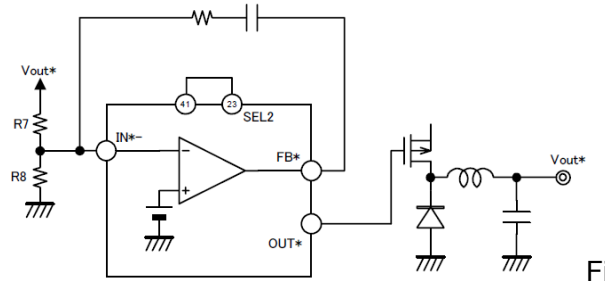


Fig.15

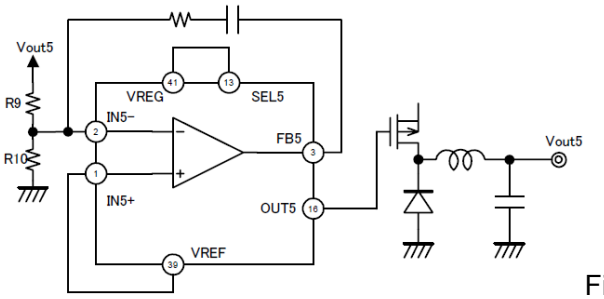


Fig.16

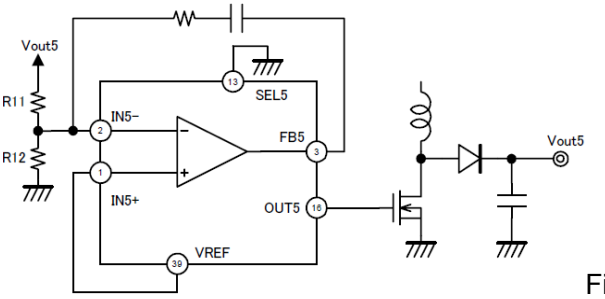


Fig.17

(9) Protect from negative voltage apply

If rather large negative voltage is applied to any pins of this IC, internal parasitic elements start operating, and they may cause malfunctions. Accordingly, the negative voltage, which is applied to each terminal of the ICs, must be kept above -0.3V.

In the case of the OUT* pin, in particular, the oscillation of voltage occurring after MOSFET's turning off can be applied to the OUT* pin through MOSFET's parasitic capacitance. As a result, there is a possibility that the negative voltage is applied to the OUT* pin. If this negative voltage reaches -0.3V or below, connect an Schottky barrier diode between OUT* pin and GND as shown in Fig. 18. The Schottky barrier diode's forward direction voltage clamps the voltage applied to the OUT* pin. In this case, use the Schottky barrier diode with low voltage drop in forward direction. Other pins should be kept above -0.3 V also based on the same reasons.

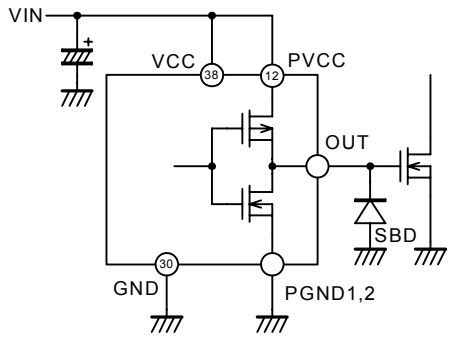


Fig.18

(10) Design of phase compensation

A switching power supply supervises output voltage with error amplifier, constitutes a closed loop, and is stabilizing voltage by negative feedback.

Phase delay with a smoothing filter and Gain with the main switching device, etc. is contained in the negative feedback circuit, and those sum totals become the phase and the gain in a closed loop.

The phase and the gain have the frequency characteristic. In a negative feedback circuit, if the gain remains 0dB or more at the frequency of 180 degrees delayed phase, a circuit will be oscillated.

In order to prevent oscillation, it is necessary to adjust the phase and the gain of error amplifier. (Fig.19) Since especially the switching power supply has repeated ON and OFF at high speed, the minute high frequency element is contained in the output, and if you setup the frequency characteristic of the error amplifier beyond necessity, it has a possibility of unstable operate and oscillate.

The gain when the phase turns 180 degrees calls gain margin, the phase when the gain becomes 0dB calls phase margin. Above 10dB of gain margin and above 50 degrees of phase margin are desirable generally and set to this condition in phase compensation. (Fig.20)

However, gain margin and phase margin against transient response (sudden change of load, etc.) are participate as trade-off, therefore when gain margin and phase margin is larger, transient response becomes margin-less condition, furthermore over shoot and under shoot of converter voltage is larger.

To determine the value of circuit components, it cannot decide here since conditions change a lot with the value of an output filter or others, but generally adjust the value between 1kΩ and 100kΩ of resistor R_{FB} and the value between 1nF and 100nF of capacitor C_{FB}. However the operation of switching power supply changes by load condition, duty cycle, temperature, etc., so when determine the value of components, examine with the real load condition in actual circuit.

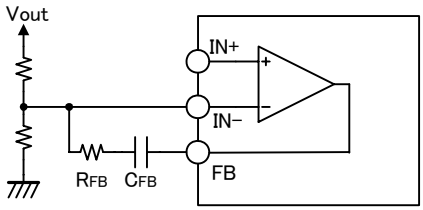


Fig.19

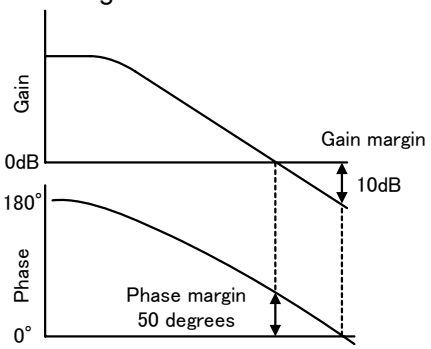
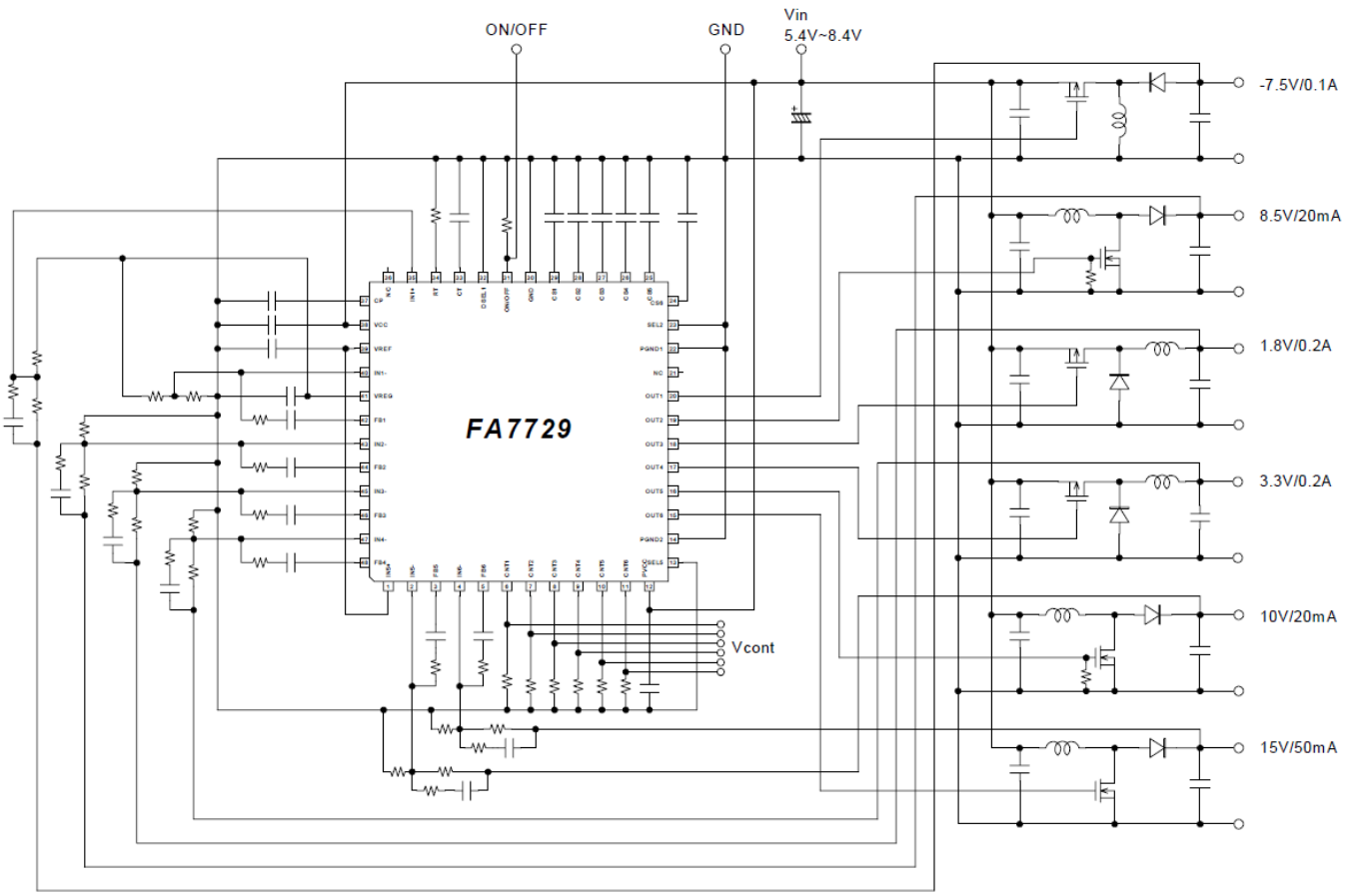


Fig.20

10. Application circuit

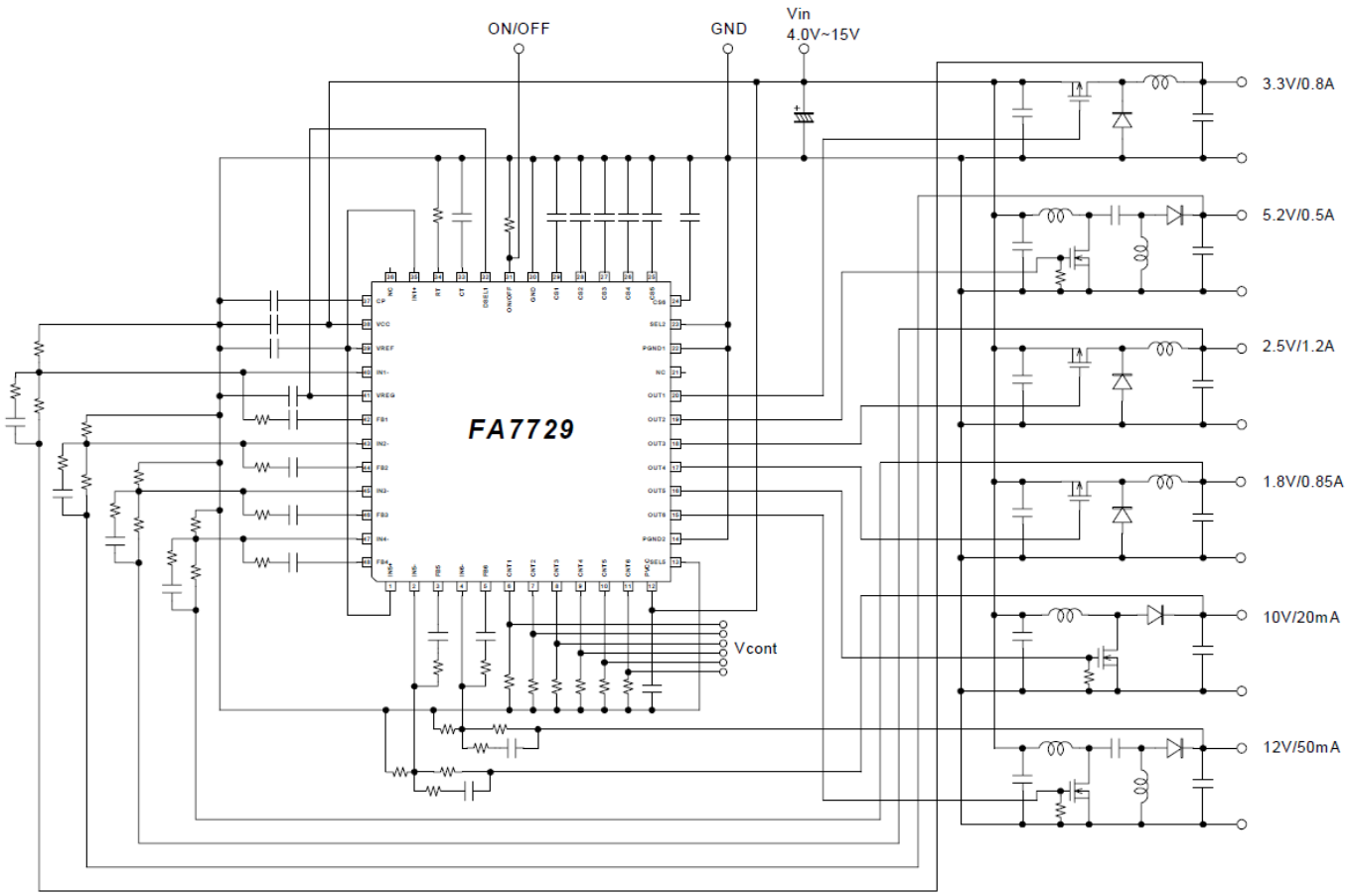
Ex.1)

OUT1	OUT2	OUT3	OUT4	OUT5	OUT6
Inverting	Boost	Buck	Buck	Boost	Boost



Ex.2)

OUT1	OUT2	OUT3	OUT4	OUT5	OUT6
Buck	Buck-Boost (SEPIC)	Buck	Buck	Boost	Buck-Boost (SEPIC)



Ex.3)

OUT1	OUT2	OUT3	OUT4	OUT5	OUT6
Invert	Buck	Buck	Buck	Buck	Boost