FUJI Power Supply Control IC

FA7738N/P

Application Note

July-2006
Fuji Electric Device Technology Co.,Ltd.

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   • Emergency equipment for responding to disasters and anti-burglary devices • Safety devices

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   • Space equipment • Aeronautic equipment • Atomic control equipment
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7.

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Contents

Notes:
- The specifications in this document are subject to change without prior notice for enhancement and other modifications.
- The example of an applied circuit and the component constant specified in this document are intended to provide assistance in design only, and do not give sufficient consideration to part dispersions or operating conditions. Users of this document should therefore establish designs while considering said part dispersions and operating conditions.

1. Overview

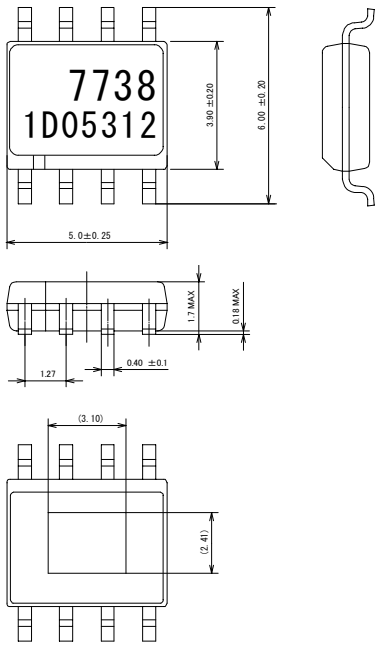
The FA7738N/P is a single-channel step-down DC-DC converter containing power MOSFET. Featuring a high-withstand-voltage process, this unit is ideally suited for use as a DC-DC converter with input voltages of up to 45 V and output currents of up to 1.5 A.
The control system is based on current mode, reduces the number of peripheral parts, and achieves a quick response.

2. Features

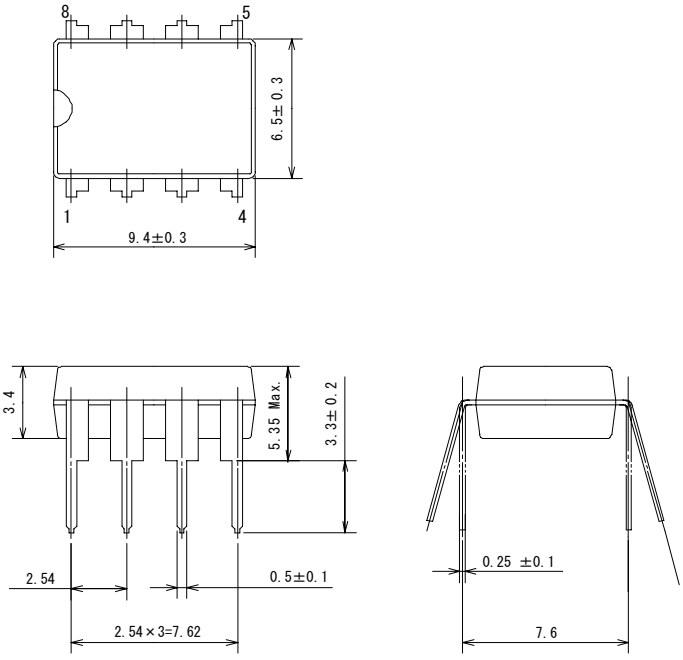
- Equipped with single-channel power MOSFET
- Efficiency as high as 85% at an output of 5 V/1.2 A (in a 200-kHz run at power input of 24 V)
- Stable control in current mode
- Switching frequency: 30 kHz to 400 kHz
- ON/OFF function: Current consumption when OFF is 0.1 mA
- Current consumption of the VCC terminal during operation is 0.5 mA
- Well-arranged protection functions:
  - Overcurrent limitation on the power MOSFET
  - Soft start (8 ms)
  - Short-circuit protection of the timer latch (90 ms delay)
  - Overheat protection
- Package: SOP-8 (E-Pad) / DIP-8

3. External dimensions

・FA7738N(SOP-8 E-Pad)

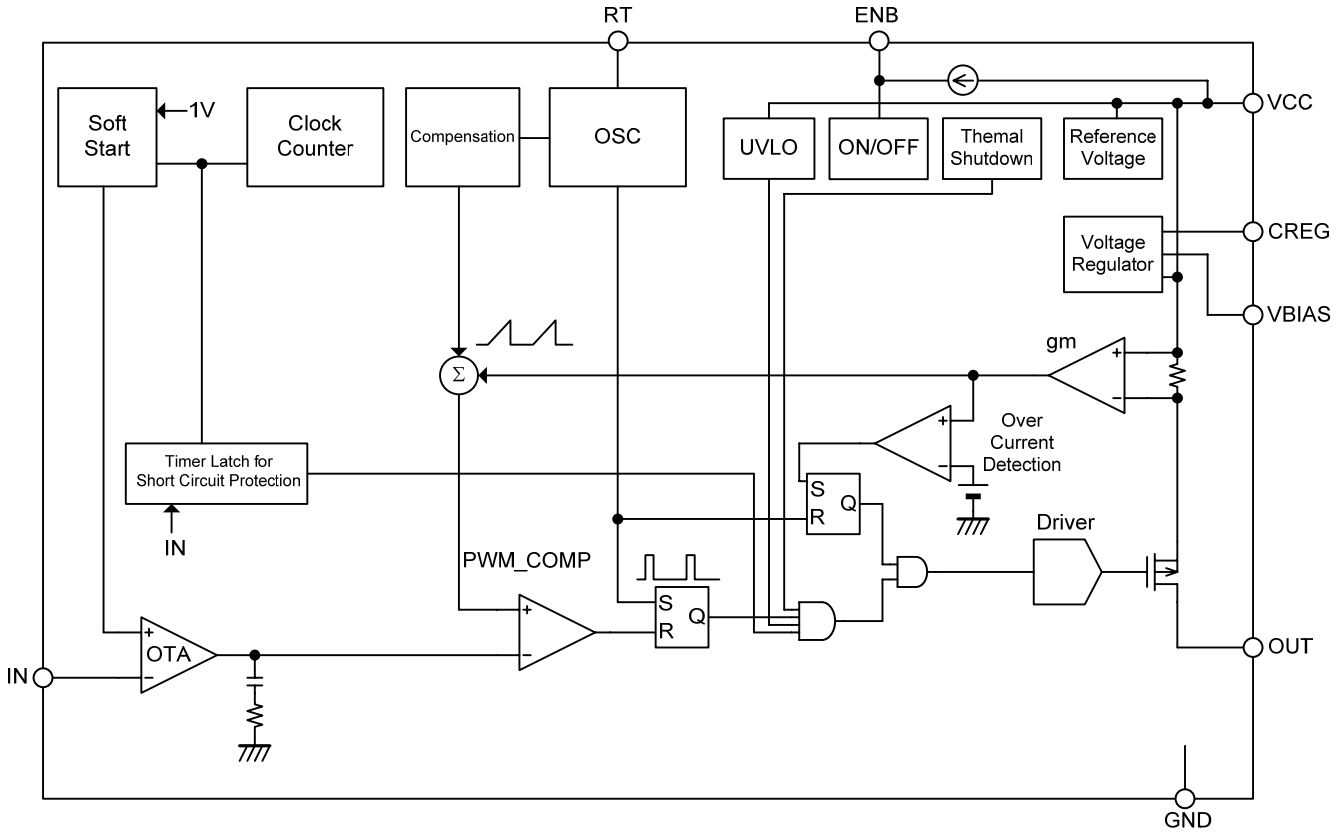


・FA7738P(DIP-8)



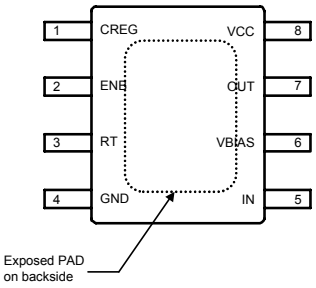
Unit:mm

4. Block diagram

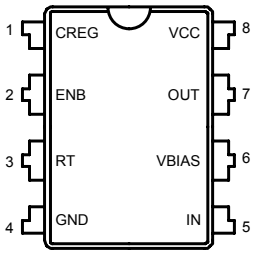


5. Description of the terminal functions

FA7738N(SOP-8 E-Pad)



FA7738P(DIP-8)



Terminal No.	Terminal code	Terminal function	Remarks
1	CREG	Internal power supply, capacitor connection terminal	Connect stabilization capacitor
2	ENB	ON/OFF control terminal (L, operation; H, open; standby mode)	
3	RT	Oscillator, timing resistance connection terminal	
4	GND	Ground terminal	
5	IN	Error amplifier reverse input	
6	VBIAS	Voltage input terminal for internal power supply VBIAS = up to 3.1 V; the internal power circuit is powered by VCC. VBIAS: 3.1 V or more; the internal power circuit is powered by output voltage.	Supplied from output voltage
7	OUT	Switching output terminal	
8	VCC	Power input	Connected bypass capacitor

6. Ratings and characteristics

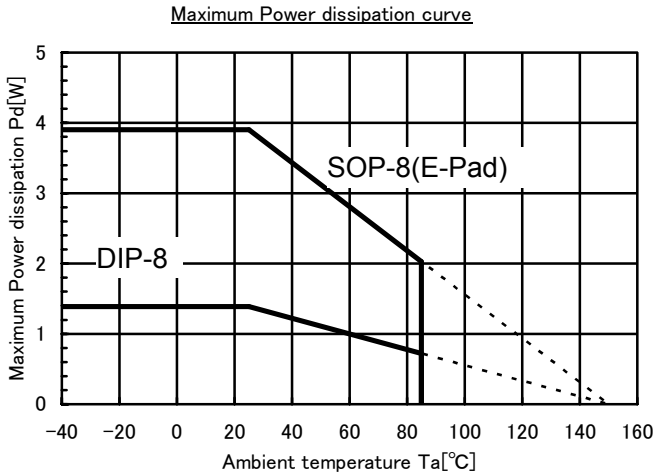
(1)Absolute maximum rating

This data is subject to change without prior notice. For details, refer to the latest version of the specifications.

*The items other than the junction temperature, operating ambient temperature, and preservation temperature are those at +25°C.

Item		Symbol	Condition	Rating	Units
Power Supply voltage (VCC)		V_{CC}		50	V
IN input voltage		V_{VIN}		-0.3 to 4.0	V
CREG input voltage		V_{CREG}		-0.3 to 4.0	V
RT input voltage		V_{RT}		-0.3 to 4.0	V
VBIAS input voltage		V_{VBIAS}		-0.3 to 6.0	V
ENB input voltage		V_{ENB}		-0.3 to 4.0	V
Power dissipation *1	SOP-8(E-Pad)	P_d	Ta≦25°C	3.9	W
	DIP-8			1.39	W
Operation junction temperature		T_J		+150	°C
Operation ambient temperature		T_{OPR}		-40 to +85	°C
Storage temperature		T_{STG}		-50 to +150	°C

Permissible loss reduction characteristic (reference value)



*1: The characteristic shall not exceed the package permissible loss (Pd).

SOP-8 (E-Pad)

When Ta is 25°C, the permissible loss is the level when a 4-layer board (50 mm x 40 mm) is mounted and the exposed pad connected by solder.

When Ta is more than 25°C, the load is rated at light SOP-8 (E-Pad) of (θj-a = 32°C/W). At such time, let θj-c = 17°C/W.

DIP-8

When Ta is 25°, the permissible loss is the level when a 2-layer board (50 mm x 4 DIP-8) is mounted.

If Ta is more than 25°C, the Pd is derated at a load reduction rate of (θj-a = 95°C/W).

At such time, let θj-c = 55°C/W.

Note: To use this IC, do so within the heat characteristic range indicated above when Tj is 150°C or less. When actually using this IC, measure the case temperature or take some other measure to ensure that Tj is 150°C or less.

(2) Recommended operating conditions

Item	Symbol	Condition	MN.	TYP.	MAX.	Units
Power Supply voltage (VCC)	V_{CC}		9		45	V
VBIAS input voltage	V_{VBIAS}		3.1		5.5	V
Oscillation frequency	f_{OSC}		30		400	kHz
CREG pin capacitance	C_{REG}		0.1	-	-	μF
VCC pin capacitance	C_{VCC}		-	0.22	-	μF
VBIAS pin capacitance	C_{VBIAS}		-	0.1	-	μF

(3) Electrical Characteristic

・The characteristics is based on the condition of V_{VCC}=42V,C_{REG}=0.1uF,R_T=39kΩ,Ta=+25°C,unless otherwise specified.

・Line regulation is the difference 45V from 9V.

(1)Regulated voltage (IN,VBIAS pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Feedback voltage	V_{IN}		0.990	1.000	1.010	V
Variation with temperature	V_{INdT}	Ta=-40 to +85°C			±1	%
Input bias current	I_{IN}	V_{IN}=0 to 2V	-0.15		0.15	μA

(2)Regulated voltage (CREG pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Regulated voltage	V_{REG}	*2		3.00		V

*2 CREG pin occurs over shoot voltage until about 4V in case of starting by ENB pin.

(3)Oscillator section (RT pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Oscillation frequency	f_{OSC}	R_T=39kΩ	102	120	138	kHz
Line regulation	f_{dV}	V_{CC}=9V to 45V		±3	±5	%
Variation with temperature	f_{dT}	Ta=-40 to +85°C		±3	±5	%

(4)Soft start section

Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Soft start time	t_S	*4	4	8	12	ms

*4 ts is 10-90% of output voltage

(5)Timer latch protection of short circuit (CP pin)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Delay time of timer latch	t_{prot}	V_{CC}=10V	45	90	180	ms
IN pin on threshold voltage	V_{THINON}	V_{CC}=10V *5-1	0.70	0.75	0.80	V
IN pin off threshold voltage	$V_{THINOFF}$	*5-2,5-3		0.85		V
IN pin Hysteresis voltage	$V_{THINHYS}$	*5-3		0.1		V

*5-1 At the IN pin, when there is a lower voltage than V_{THINON}, the counter for timer latch starts.

*5-2 At the IN pin, when there is a higher voltage than V_{THOFF}, the counter for timer latch stops.

*5-3 Design value

(6)Under voltage lockout circuit section (VCC pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
ON threshold voltage of VCC	V_{UVLOON}	IC is enabled.		6.9	8.2	V
OFF threshold voltage of VCC	$V_{UVLOOFF}$	IC is disabled.	4.9	5.9		V
Hysteresis voltage	$V_{UVLOHYS}$		0.4	1.0		V

(7)ON/OFF control section (EN pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Charge current of ENB	I_{ENB}	V_{ENB}=0V		10	15	μA
ON threshold voltage of ENB	V_{ENBON}	IC is enabled			1	V
OFF threshold voltage of ENB	V_{ENBOFF}	IC is disabled *7	2			V

*7 Normally ENB pin is open, this terminal voltage is fixed at about 5V, for input voltage for this terminal is not necessary.

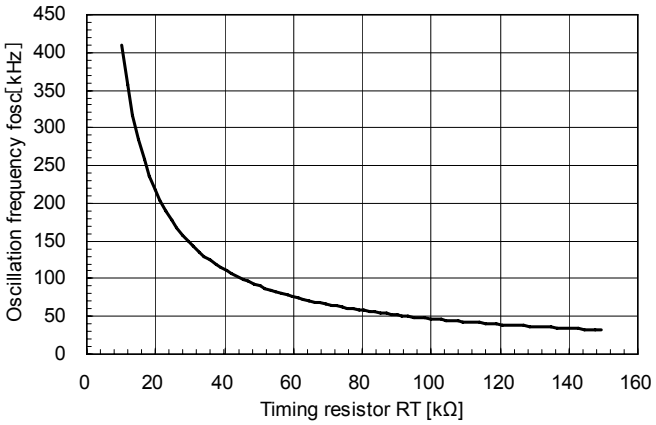
(8)Thermal shutdown section						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Thermal shutdown on	T_{OHPON}	Output is disabled	125	135		°C
Thermal shutdown off	T_{OHPON}	Output is enabled		115		°C
Thermal shutdown hysteresis	T_{OHPHYS}			20		°C

(9)Output section (OUT pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
High side on resistance	R_{ONP}	V_{CC}=10V, I_{DS}=1.0A		0.8	1.0	Ω
		Ta=85°C V_{CC}=10V, I_{DS}=1.0A		1.2	1.5	Ω
Current limit	I_{OLMT}		2.5	4	5.5	A

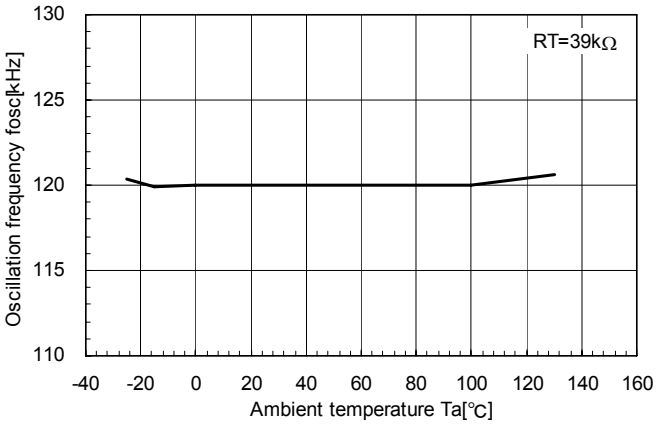
(10)Overall section (VCC,VBIAS pin)						
Item	Symbol	Condition	MIN.	TYP.	MAX.	Units
Supply current (VCC)	I_{CCVCC}	Switching at non-load (at VBIAS<3.1V)		0.75	1.5	mA
		Switching at non-load (at VBIAS>3.1V)		0.4	1.0	
	$I_{CCSTBVCC}$	Stand by (ENB=open)		50	100	μA
Supply current (VBIAS)	$I_{CCVBIAS}$	Switching at non-load (at VBIAS<3.1V)		0	20	μA
		Switching at non-load (at VBIAS>3.1V)		0.4	0.7	mA
	$I_{CCSTBVBIAS}$	Stand by (ENB=open)		0	20	μA

7. Characteristic curves

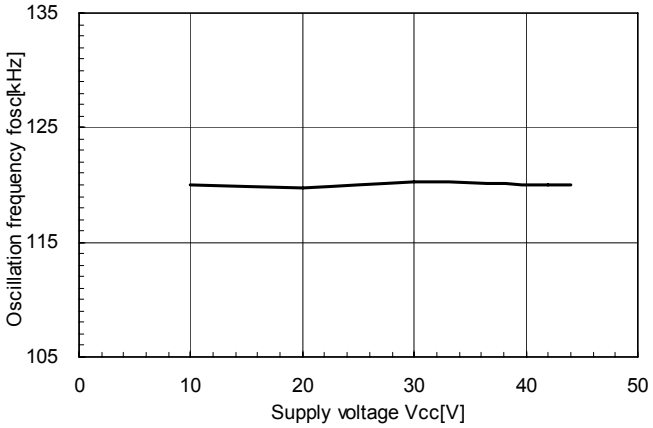
Timing resistor vs. Oscillation frequency



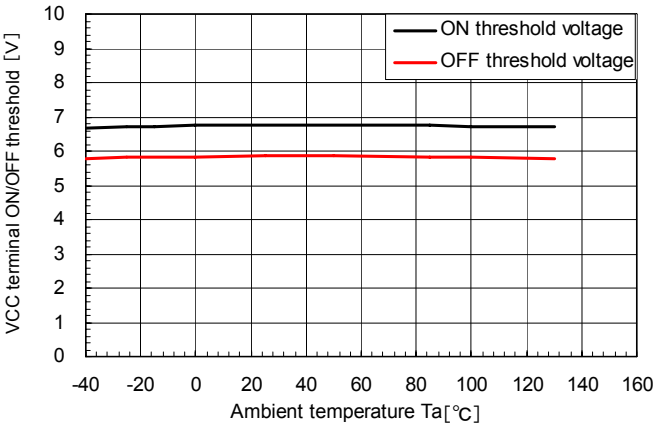
Oscillation frequency vs.ambient temperature



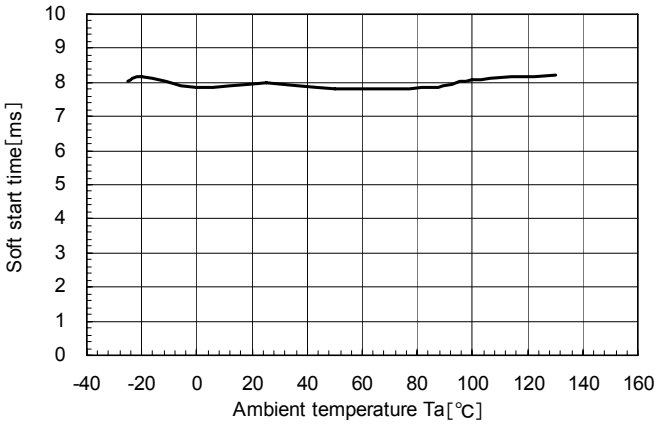
Oscillation frequency vs. Supply voltage VCC



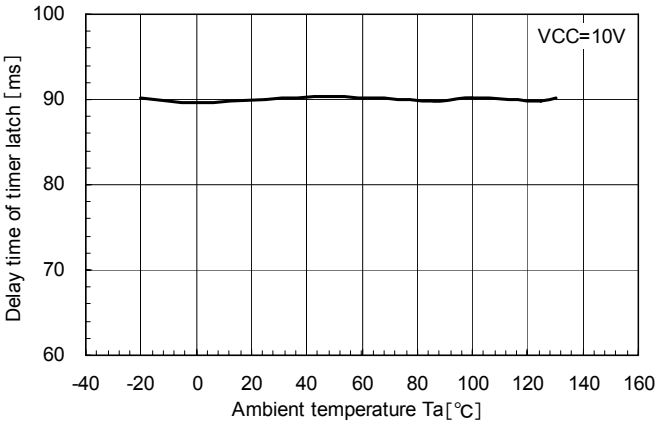
Under voltage lockout vs.Ambient temperature



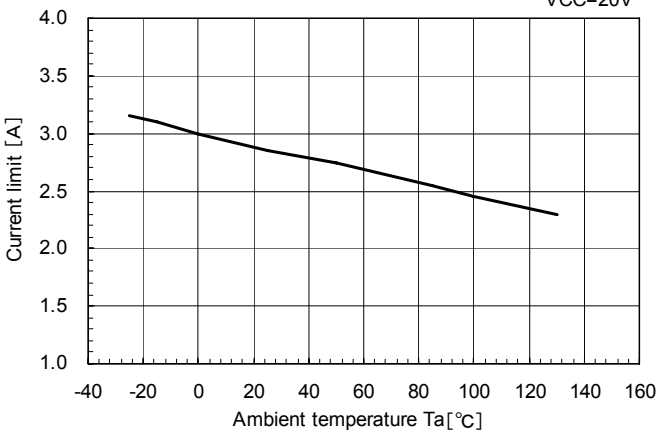
Soft start time vs.Ambient temperature



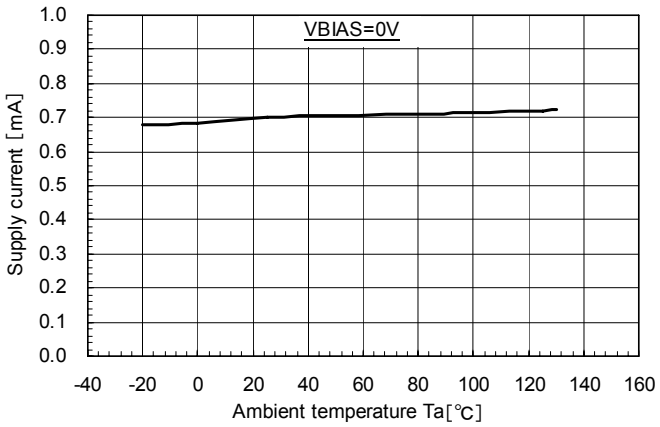
Delay time of timer latch vs.Ambient temperature



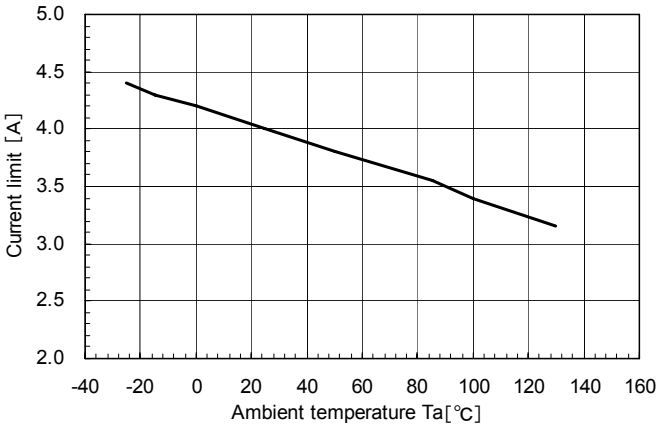
Current limit vs.Ambient temperature VCC=20V



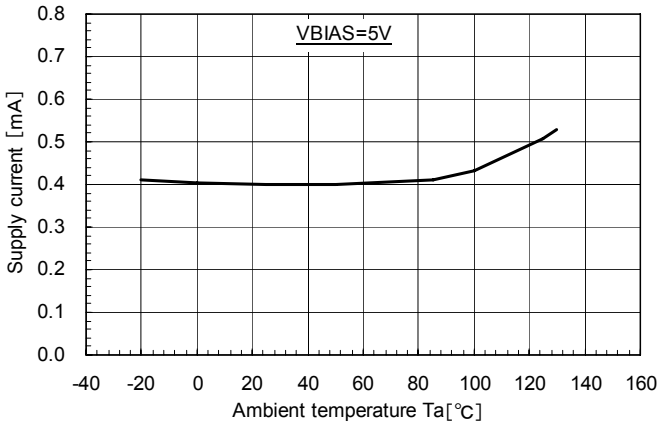
Supply current vs.Ambient temperature VBIAS=0V



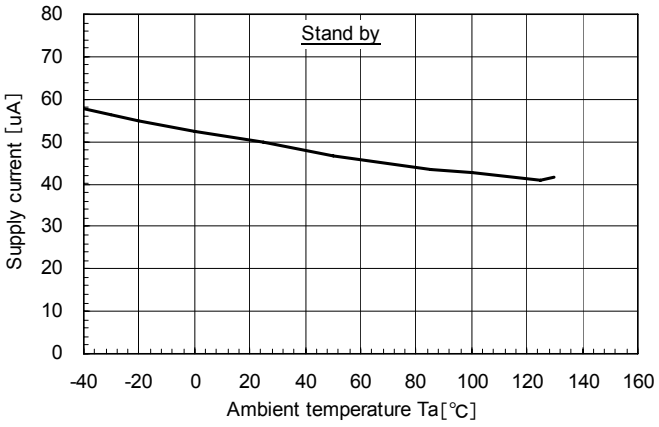
Current limit vs.Ambient temperature VCC=40V



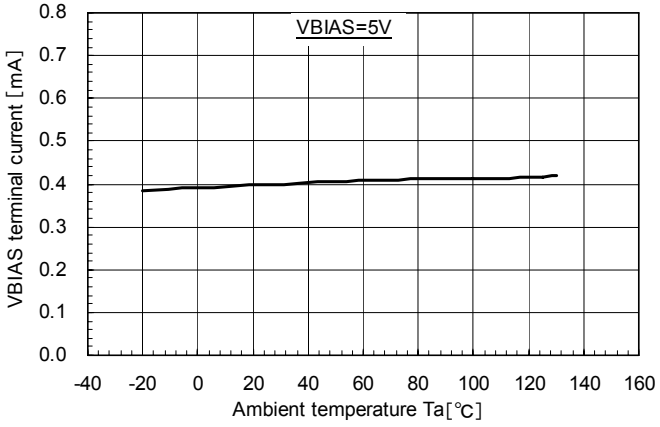
Supply current vs.Ambient temperature VBIAS=5V



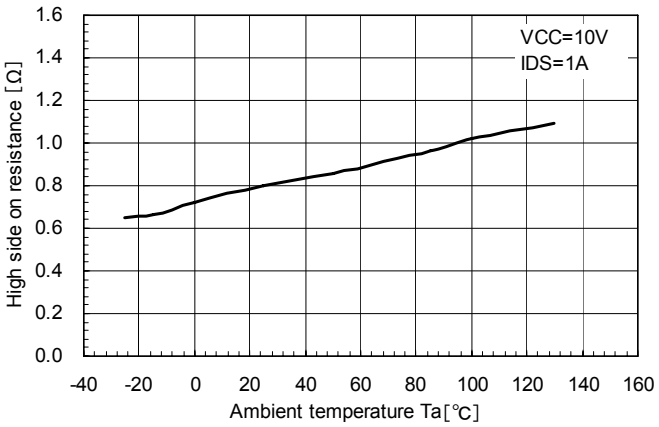
Supply current vs.Ambient temperature Stand by



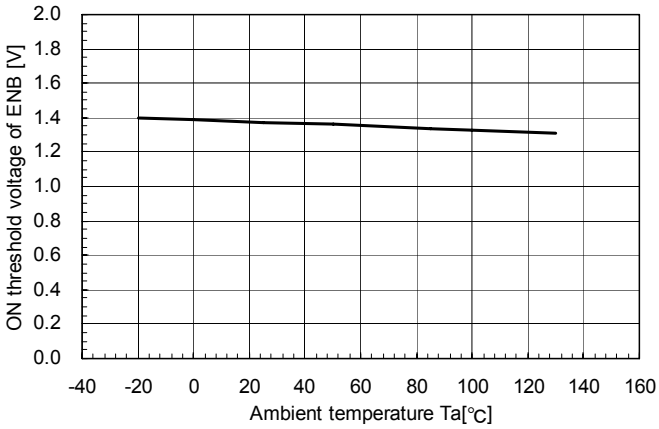
VBIAS terminal current vs.Ambient temperature VBIAS=5V



High side on resistance vs.Ambient temperature



ON threshold voltage of ENB vs.Ambient temperature



8. Operation description of each block

(1) Reference voltage circuit

The reference voltage circuit generates an output return voltage (VIN) of 1.00 V ± 1% for which temperature compensation is provided by the VCC voltage, along with an internal control power (VREG) of 3.0 V.

The output return voltage (VIN) is connected to the non-reverse input of the error amplifier (OTA) and constitutes the reference voltage of the error amplifier.
The power VREG voltage supply of the internal control system is output from the CREG terminal and is connected with the capacitor CREG for stabilization.
This voltage is designed specifically for the control power of all IC internal circuits. It therefore cannot be used as an external stabilization power supply.
To connect the CREG capacity of the stabilization capacitor to the CREG terminal, see the recommended operating conditions.

(2) Oscillator

This oscillator is based on capacitor charge and discharge. Its oscillation frequency can be set to a desired level based on the RT of the resistor to be connected to the RT terminal (Fig. 1).
(A high RT means a low operating frequency.
A low RT means a high operating frequency.)
Set the oscillation frequency to any setting between 30 kHz and 400 kHz.
The RT terminal outputs DC voltage of about 1 V.

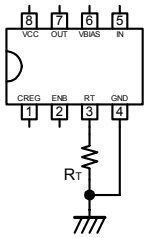


Fig.1

(3) Error amplifier (OTA)

The IN terminal (No. 5) is a reverse input terminal. The non-reverse input is connected to a reference voltage (VIN) with 1.0 V ± 1% inside the IC. The FB terminal is not exposed outside and performs phase compensation inside the IC.
Voltage is supplied to the IN terminal as a resistance-divided voltage from the output voltage of the DC-DC converter circuit. The output voltage Vout of the DC-DC converter can be determined by:

$$Vout = \frac{R1 + R2}{R2} \times V_{IN}$$

Note that, if the unit does not operate stably depending on the input conditions, capacitor C1 can be connected to it for phase adjustment and enhancement.

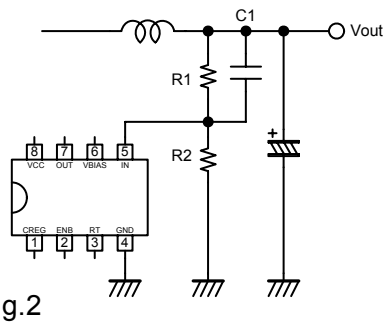


Fig.2

(4) PWM comparator

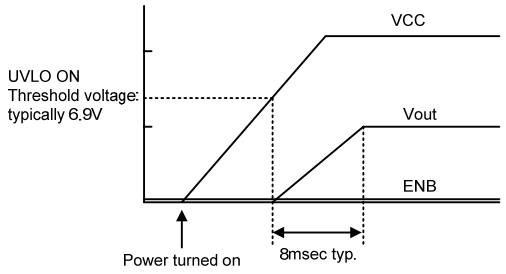
The ON state of output (from the OUT terminal) starts with the ON signal of the oscillator. It is turned off when the coil current reaches the level specified by the output (OTA output) of the error amplifier.

(5) Soft starter

This unit incorporates a soft starter to prevent the DC-DC converter circuit from anomalous operation (such as a rush current) at startup.
A soft start is made by gradually increasing the output by progressively raising the reference voltage of the error amplifier (OTA).

The soft start time is fixed at 8 msec (typically) inside the IC.
This refers to the time from when power is turned on to when the input voltage reaches the ON threshold voltage (typically 6.9 V) or more of the low-voltage malfunction prevention circuit (Fig. 3).
Once power is supplied, an ENB signal initiates a soft start.

Power supply startup from when the ENB signal is set to low state



Startup by an ENB signal

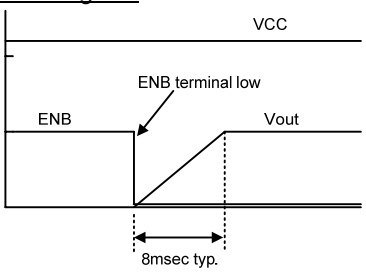


Fig. 3

(6) Short-circuit protection circuit for the timer latch

This unit incorporates a short-circuit protection function for the timer latch that stops switching if the output voltage remains low for a certain time due to an output short-circuit or other trouble occurring in the DC-DC converter circuit.

If the output voltage goes low due to an output short-circuit or other trouble occurring in the DC-DC converter circuit, the IN terminal of the reverse input of the error amplifier will also go low. This voltage is detected as 0.75 V (typically) or less, thus activating the timer latch counter. If a state of insufficient output voltage continues unresolved and exceeds delay time tprot (typically 90 msec) for protecting against a timer latch short circuit, the unit will judge the state as an error,

stop switching, and protect the circuit (Fig. 4).

The delay time for protecting the timer latch against a short circuit is fixed inside the IC and cannot be configured from outside.

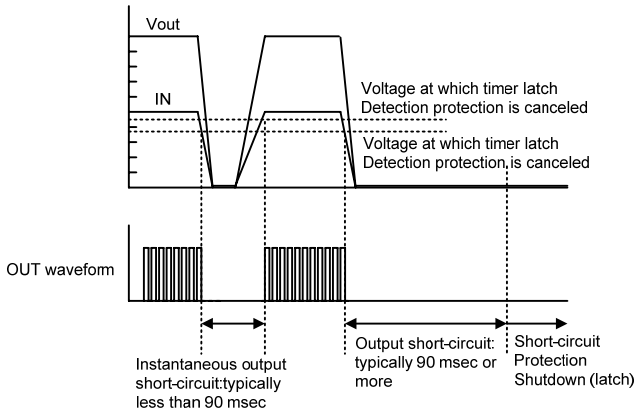


Fig. 4

Recovering from latch stoppage requires resetting by using an ENB terminal or setting the input voltage to a level lower than the UVLO voltage.

(7) Overcurrent limitation circuit

The system incorporates a pulse-by-pulse overcurrent limitation function that detects and limits each main circuit current peak value of the internal MOSFET.

The current that flows through the internal MOSFET enters an overcurrent protection comparator as a voltage signal based on the internal detection resistor. If this signal is higher than the reference voltage, the internal MOSFET is turned off and limited so that no further current will flow. This limitation will be reset in the next cycle with its output turned on again. This limitation will be repeated in each cycle along with overcurrent limitation.

If the overcurrent state becomes even heavier and the output voltage drops to a level lower than 75% (typically) due to line impedance or some other factor, the system will function in the same way as timer latch short-circuit protection described in (6) and be shut down.

(8) Overheat protection circuit

The system incorporates an overheat protection function that stops switching if the IC overheats due to overcurrent or other error.

If the IC chip reaches 135°C (typically), the system stops switching. If the chip temperature falls to 115°C, the system will resume switching. At such time, the system will stop output, but the latching function will not work.

(9) ON/OFF controller

Turning the output on and off is possible by applying external signal from the ENB terminal.

To turn the output on, the ENB terminal can be set to less than 1.0 V to initiate switching. At such time, a soft start gradually increases the output voltage (Fig. 3).

The output can be turned off by either opening the ENB terminal or applying an external voltage of at least 2 V.

When the ENB terminal is open, the ENB terminal will reach a voltage of about 5 V.

At such time, the IC will enter standby status, with the internal control voltage (typically 3.0 V) shut down, so that current consumption of the IC will reach a maximum of 100 μA.

(10) Low-voltage malfunction prevention circuit (UVLO)

The system incorporates a low-voltage malfunction prevention circuit to prevent circuit malfunction in case of a drop in power supply voltage.

Increasing the power supply voltage from 0 V will cause the system to start running at a Vcc of 6.9 V (typically). When the power supply voltage is low, the output will be shut down at a Vcc of 5.9 V (typically).

(11) Output circuit

The output circuit consists of P channel MOSFET, with ON resistance of 0.8 Ω (typically).

(12) VBIAS circuit

The system incorporates VBIAS terminal to increase the efficiency of the power supply circuit and reduce IC loss. The internal power supply circuit of most ICs is generated by voltage supplied by the VCC voltage. The resulting output voltage of the power supply circuit can be returned to the VBIAS terminal to keep the voltage source for generating an internal power supply at a low level, thus enabling operation at lower power consumption (Fig. 5).

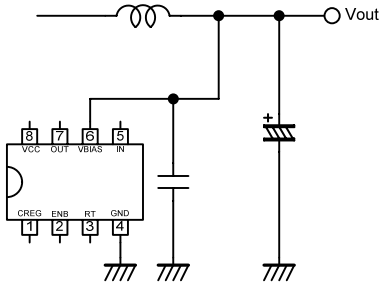


Fig. 5

When no VBIAS terminal is used, the operating current consumption of the VCC terminal is 0.75 mA (typically). When a VBIAS terminal is used, the comparable consumption is 0.4 mA(typically).

This operation switchover is performed when the VBIAS terminal voltage (i.e., output voltage of the power supply circuit) is 3.1 V. Therefore, said operation will be effective only when the output voltage of the power supply circuit is more than 3.1 V.

Moreover, the VBIAS terminal incorporates a 5.5 V Zener diode for protection. This ensures that, if voltage of more than 5.5 V is applied to the VBIAS terminal, a current will be applied to the Zener diode, resulting in a rise in the loss.

Therefore, use the power supply circuit with an output voltage between 3.1 V and 5.5 V when using the VBIAS terminal.

When no VBIAS terminal is used (with the power supply circuit having an output voltage less than 3.1 V or more than 5.5 V), connect the VBIAS terminal to GND (Fig. 6).

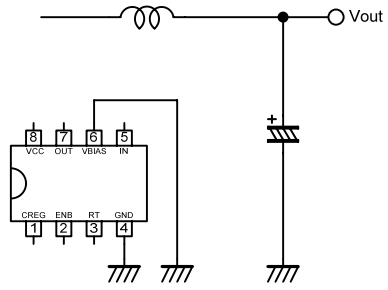


Fig. 6

When a VBIAS terminal is used, connect a ceramic capacitor close to the VBIAS terminal as shown in Fig. 5 to eliminate noise (about 0.1 μF is recommended).

8. Design tips

(1) Setting an oscillation frequency

An oscillation frequency can be adjusted to a desired level by changing the value of the resistor connected to the RT terminal as described under item (2) in "Operation description of each block." Set an oscillation frequency between 30 kHz and 400 kHz.

The oscillation frequency with regard to the RT can be determined by the "Timing resister vs. Oscillation frequency" of the characteristic curve or roughly determined by using the following equation:

$$fosc = 3738 \times R_T{}^{-0.95}$$

Where, *fosc*: Oscillation frequency [kHz]
RT: Timing resistance [kΩ]

Note that this equation provides a guide for setting a rough level and is not intended to guarantee that level. The operating frequency is determined by the characteristic dispersion and noise of the IC, along with external parts and other conditions. In determining a constant, conduct an operation check during actual setting.
The RT terminal is a high-impedance terminal and vulnerable to noise. Therefore, connect the timing resistor RT to a position close to the RT terminal and GND terminal by short wiring.

(2) IC losses

This IC incorporates a switching MOSFET. The loss generated in this MOSFET accounts for most of the IC loss, and the loss is largely determined by the input/output conditions of the power supply circuit. When using this IC, be very careful not to let it exceed the permissible loss of the IC (SOP-8 E-Pad: 3.9 W at 25°C, DIP-8: 1.39 W at 25°C). Note also that the permissible loss in SOP-8 (E-Pad) specified in this document is a condition for mounting a 4-layer board (50 mm x 40 mm) at Ta of 25°C when the exposed pad is connected by solder. Note that the loss will be smaller than the permissible loss specified above if any other board (such as 2-layer board) is used or the exposed pad is unconnected.

Depending on the input voltage and operating ambient temperature, the recommended maximum load current for the DC-DC converter consisting of SOP-8 (E-Pad) of this IC is about 1.5 A.

(3) Constraints and recommended operating conditions for external parts

For stable operation, set the constants, applied voltages, and currents of the parts to be connected to each terminal of this IC within the recommended range of operating conditions.

The system incorporates a PchMOSFET between the OUT terminal and the VCC terminal. This PchMOSFET furnishes a parasitic diode. Therefore, current will flow from the OUT terminal to the VCC terminal if the OUT terminal voltage exceeds the Vcc voltage.

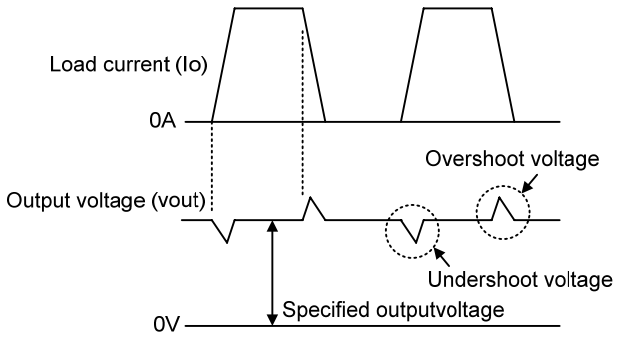
(4) Preventing the application of negative voltage

Applying a high negative voltage to each terminal of the IC activates the parasitic devices in the IC, and may result in a malfunction. Make sure that no terminal is subjected to voltage of less than -0.3 V.

(5) Improving the transient response characteristic

The transient response characteristic of a power supply circuit generally refers to overshoot in the output voltage when the power supply voltage is started, and to overshoot/undershoot in the output voltage when the load current changes abruptly (Fig. 7).

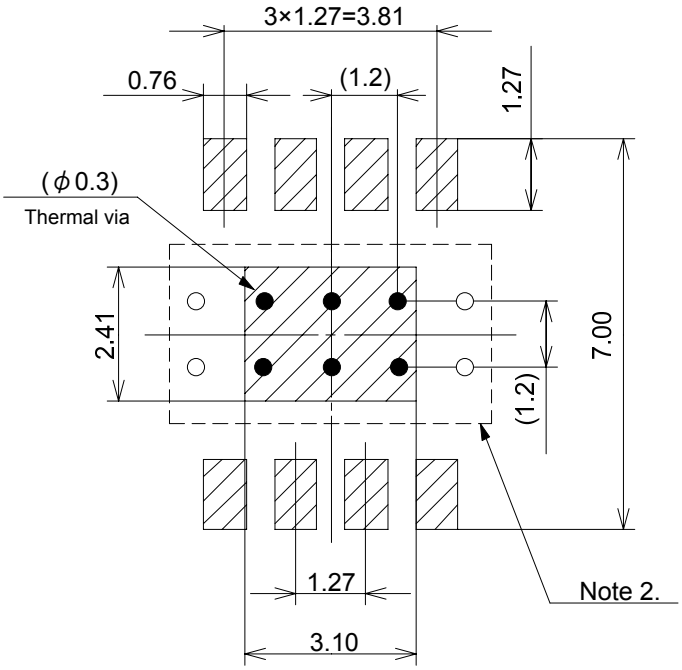
This IC undergoes hardly any overshoot at startup due to the soft start of the reference voltage. However, the overshoot/undershoot may occur when the load changes abruptly, depending on the conditions. This overshoot/undershoot can be restricted by connecting a capacitor to the output voltage detection resistor as shown in Fig. 2.
No universal constant can be determined because it varies with the conditions. However, we believe that an appropriate effect can be produced when the constant is between hundreds of pico-Farads and tens of nano-Farads.



(6) Mounting SOP-8 (E-Pad)

Install the SOP-8 (E-Pad) package of this IC by providing a 4-layer board on which to mount components for reducing the thermal resistance of the package, along with a GND pattern in the intermediate layer of the board, and connect the package E-Pad by using a thermal via.

Fig. 8 shows a recommended foot pattern.

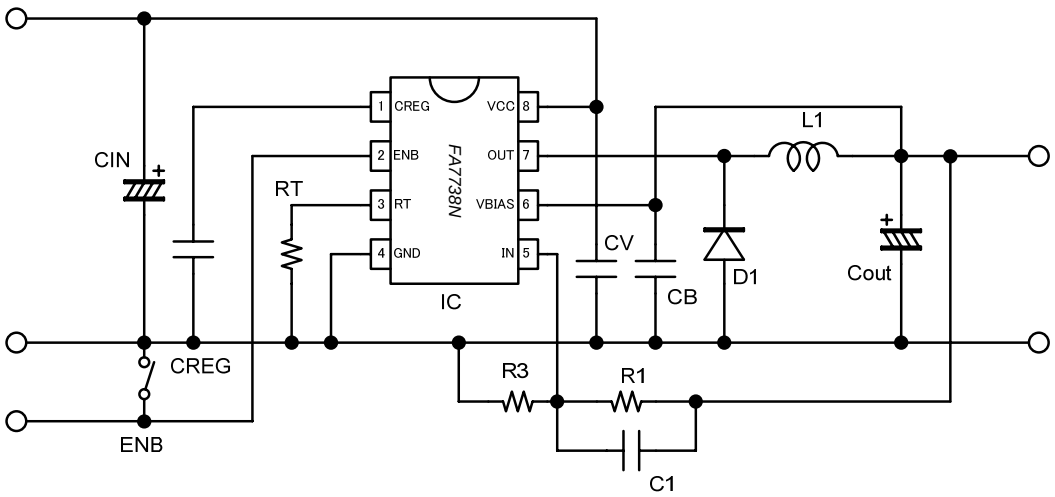


Notes:

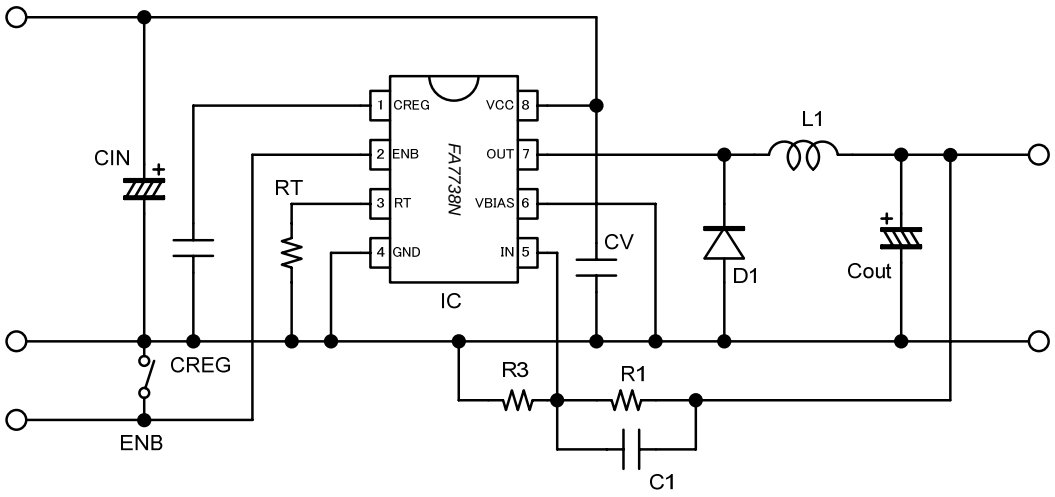
1. The exposed pad pattern conforms to JEDEC JESD51-5.
2. The resist is the same as that of the exposed pad. A thermal via should also be installed in positions other than the resist opening.

10. Example of an applied circuit

(1) Output voltage is between 3.1V and 5.5V.



(2) Output voltage is less than 3.1V or more than 5.5V.



When determining values and external discrete components, examine under the actual circuit condition.

11. Example of representative characteristics

(1)Input voltage：20～30V, Output voltage：5V

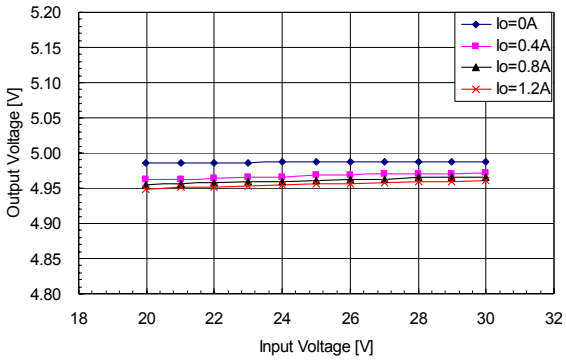
・Parts list

Ref.	Description	Type name	Maker
IC	IC	FA7738N	Fuji
D1	Schottky Diode	SD833-06	Fuji
L1	Inductor	CDRH104R-47uH	SUMIDA
CIN	Electrolytic Capacitor	220uF/35V	Panasonic
Cout	Electrolytic Capacitor	220uF/6.3V	Panasonic
CREG	Ceramic Capacitor	0.1uF	

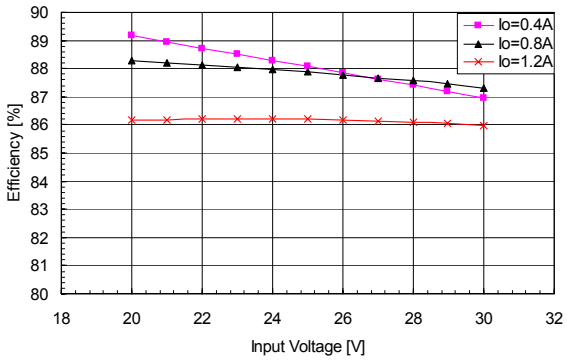
Ref.	Description	Type name	Maker
CV	Ceramic Capacitor	0.1uF	
CB	Ceramic Capacitor	0.1uF	
C1	Ceramic Capacitor	220pF	
RT	Resistor	22kΩ(fosc=200kHz)	
R1	Resistor	40kΩ	
R3	Rsisitor	10kΩ	

・Typical Operating Characteristics

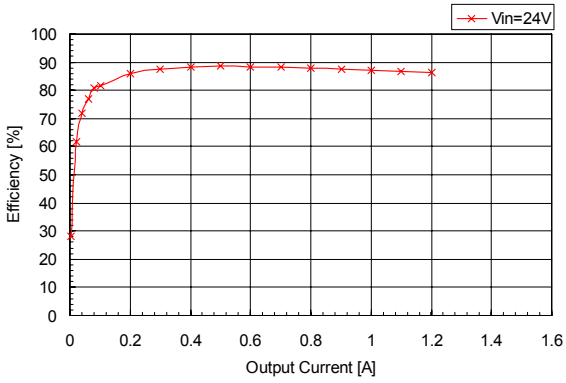
Output Voltage vs.Input Voltage



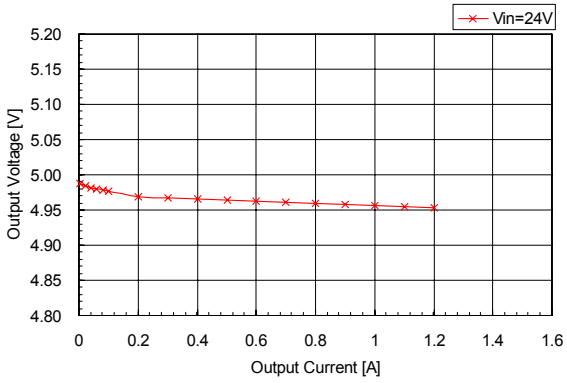
Efficiency vs. Input Voltage



Efficiency vs. Output Current



Output Voltage vs. Output Curent



(2)Input voltage：20～30V, Output voltage：3.3V

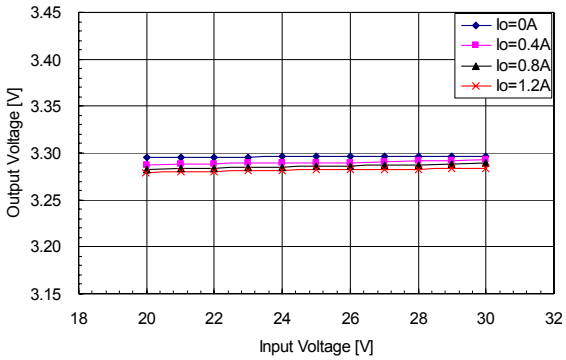
・Parts list

Ref.	Description	Type name	Maker
IC	IC	FA7738N	Fuji
D1	Schottky Diode	SD833-06	Fuji
L1	Inductor	CDRH104R-47uH	SUMIDA
CIN	Electrolytic	220uF/35V	Panasonic
Cout	Electrolytic	220uF/6.3V	Panasonic
CREG	Ceramic	0.1uF	

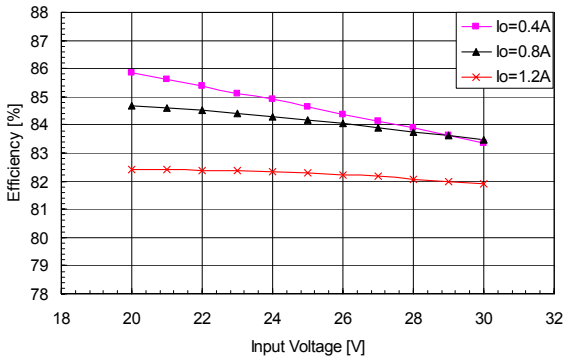
Ref.	Description	Type name	Maker
CV	Ceramic	0.1uF	
CB	Ceramic	0.1uF	
C1	Ceramic	220pF	
RT	Resistor	22kΩ(fosc=200kHz)	
R1	Resistor	23kΩ	
R3	Rsisitor	10kΩ	

・Typical Operating Characteristics

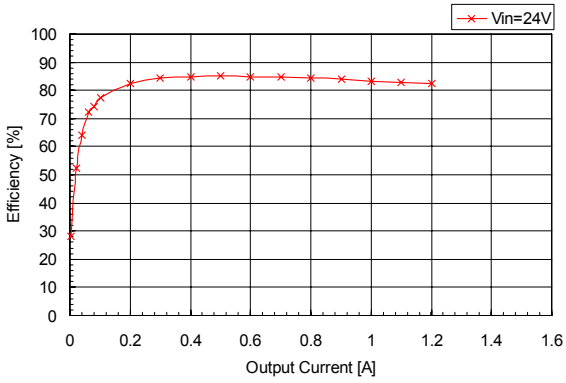
Output Voltage vs.Input Voltage



Efficiency vs. Input Voltage



Efficiency vs. Output Current



Output Voltage vs. Output Curent