

FML16N60ES

FUJI POWER MOSFET

Super FAP-E³ series

N-CHANNEL SILICON POWER MOSFET

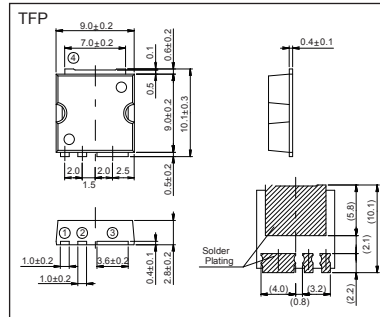
Features

- Maintains both low power loss and low noise
- Lower R_{DS(on)} characteristic
- More controllable switching dv/dt by gate resistance
- Smaller V_{GS} ringing waveform during switching
- Narrow band of the gate threshold voltage (4.2±0.5V)
- High avalanche durability

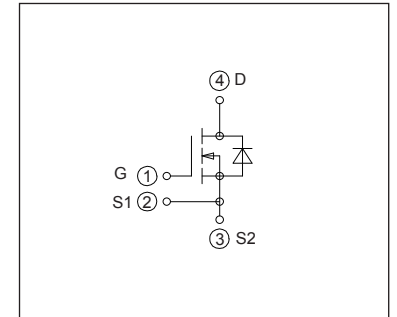
Applications

- Switching regulators
- UPS (Uninterruptible Power Supply)
- DC-DC converters

Outline Drawings [mm]



Equivalent circuit schematic



Maximum Ratings and Characteristics

Absolute Maximum Ratings at T_c=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks
Drain-Source Voltage	V _{DS}	600	V	
	V _{DSX}	600	V	V _{GS} = -30V
Continuous Drain Current	I _D	±16	A	
Pulsed Drain Current	I _{DP}	±64	A	
Gate-Source Voltage	V _{GS}	±30	V	
Repetitive and Non-Repetitive Maximum Avalanche Current	I _{AR}	16	A	Note*1
Non-Repetitive Maximum Avalanche Energy	E _{AS}	554.8	mJ	Note*2
Repetitive Maximum Avalanche Energy	E _{AR}	27	mJ	Note*3
Peak Diode Recovery dv/dt	dv/dt	3.8	kV/μs	Note*4
Peak Diode Recovery -di/dt	-di/dt	100	A/μs	Note*5
Maximum Power Dissipation	P _D	1.44	W	T _a =25°C
		270		T _c =25°C
Operating and Storage Temperature range	T _{ch}	150	°C	
	T _{stg}	-55 to +150	°C	

Electrical Characteristics at T_c=25°C (unless otherwise specified)

Description	Symbol	Conditions	min.	typ.	max.	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	I _D =250μA, V _{GS} =0V	600	-	-	V
Gate Threshold Voltage	V _{GS} (th)	I _D =250μA, V _{DS} =V _{GS}	3.7	4.2	4.7	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	-	-	25	μA
		V _{DS} =480V, V _{GS} =0V	-	-	250	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	-	10	100	nA
Drain-Source On-State Resistance	R _{DS} (on)	I _D =8A, V _{GS} =10V	-	0.40	0.47	Ω
Forward Transconductance	g _{fs}	I _D =8A, V _{DS} =25V	5	10	-	S
Input Capacitance	C _{iss}	V _{DS} =25V	-	2100	3150	pF
Output Capacitance	C _{oss}	V _{GS} =0V	-	230	345	
Reverse Transfer Capacitance	C _{rss}	f=1MHz	-	13	19.5	
Turn-On Time	td(on)	V _{CC} =300V	-	43	64.5	ns
	tr	V _{GS} =10V	-	41	61.5	
Turn-Off Time	td(off)	I _D =8A	-	94	141	
	tf	R _G =18Ω	-	20	30	
Total Gate Charge	Q _G	V _{CC} =300V	-	56	114	nC
Gate-Source Charge	Q _{GS}	I _D =16A	-	20	25.5	
Drain-Source Crossover Charge	Q _{SW}	V _{GS} =10V	-	21	33	
Gate-Drain Charge	Q _{GD}		-	9.5	14.5	
Avalanche Capability	I _{AV}	L=1.74mH, T _{ch} =25°C	16	-	-	A
Diode Forward On-Voltage	V _{SD}	I _F =16A, V _{GS} =0V, T _{ch} =25°C	-	0.90	1.08	V
Reverse Recovery Time	trr	I _F =16A, V _{GS} =0V	-	0.7	-	μS
Reverse Recovery Charge	Q _{RR}	-di/dt=100A/μs, T _{ch} =25°C	-	9	-	μC

Thermal Characteristics

Description	Symbol	Test Conditions	min.	typ.	max.	Unit
Thermal resistance	R _{th} (ch-c)	Channel to case			0.46	°C/W
	R _{th} (ch-a)	Channel to Ambient			87	°C/W
	R _{th} (ch-a)	Channel to Ambient Note*6			52	°C/W

Note *1 : T_{ch}≤150°C

Note *2 : Stating T_{ch}=25°C, I_{AS}=5A, L=33.8mH, V_{CC}=50V, R_G=10Ω,

E_{AS} limited by maximum channel temperature and avalanche current.

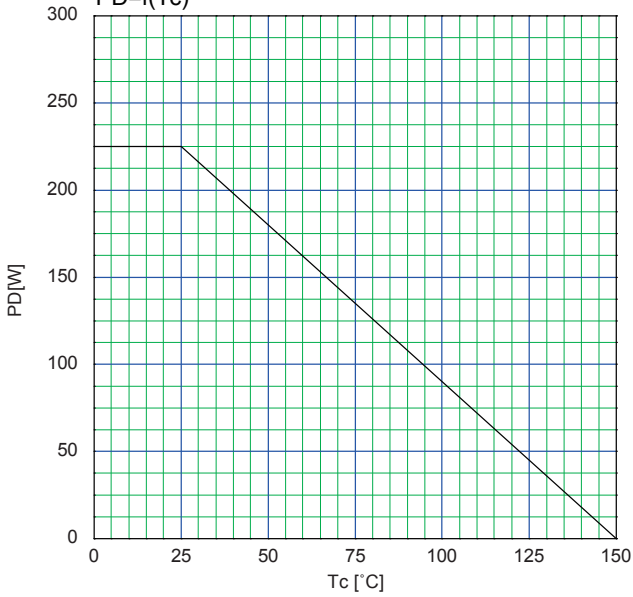
Note *3 : Repetitive rating : Pulse width limited by maximum channel temperature.

Note *4 : I_F≤I_D, -di/dt=100A/μs, V_{CC}≤BV_{DSS}, T_{ch}≤150°C.

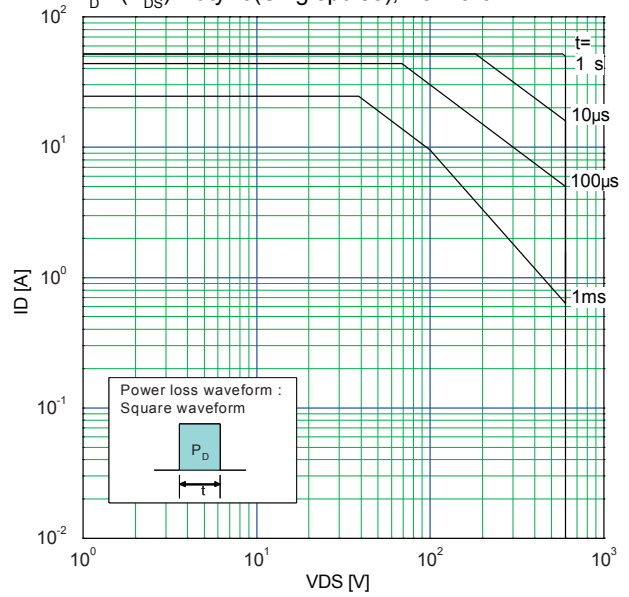
Note *5 : I_F≤I_D, dv/dt=6.3kV/μs, V_{CC}≤BV_{DSS}, T_{ch}≤150°C.

Note *6 : Surface mounted on 1000mm², t=1.6mm FR-4 PCB (Drain pad area : 500mm²)

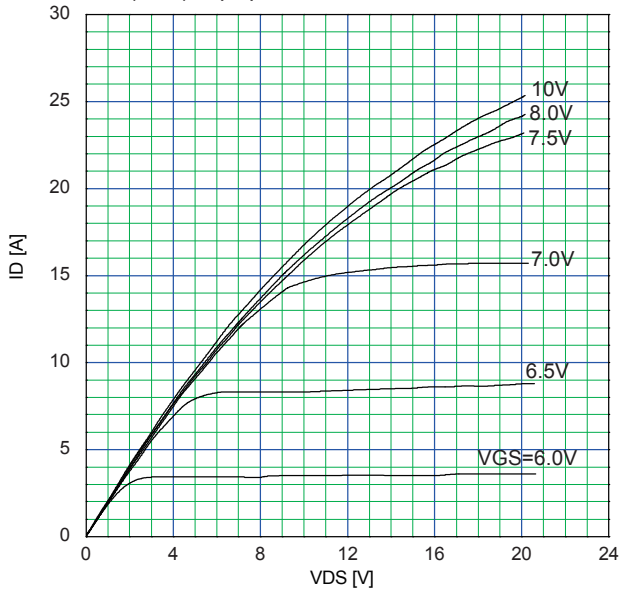
Allowable Power Dissipation
 $P_D=f(T_c)$



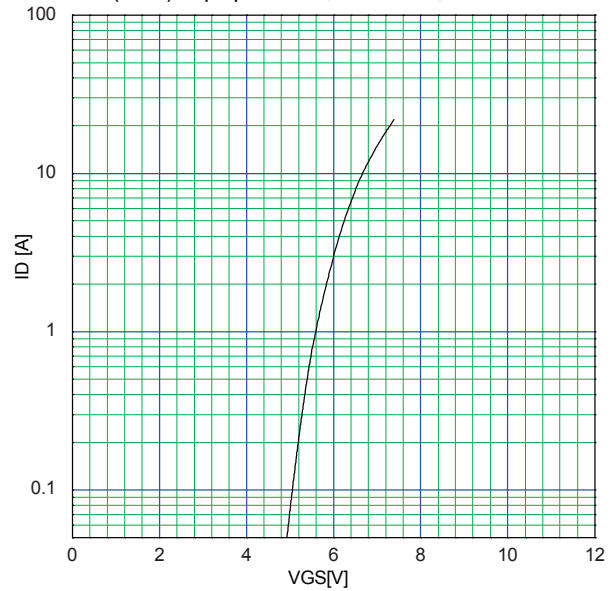
Safe Operating Area
 $I_D=f(V_{DS}): \text{Duty}=0(\text{Single pulse}), T_c=25^\circ\text{C}$



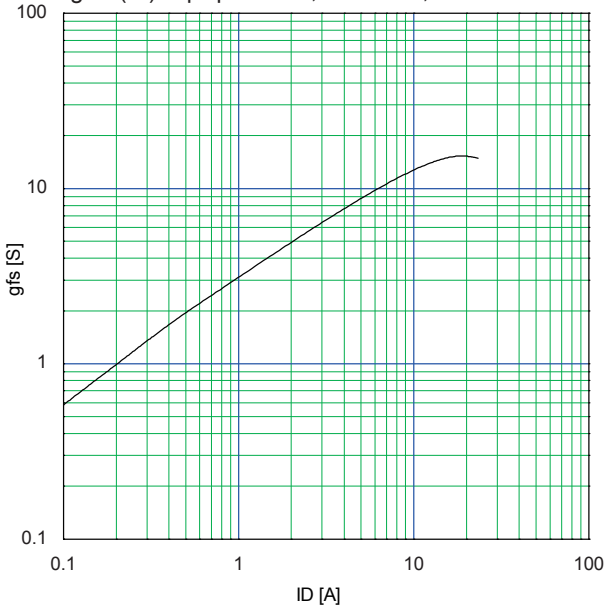
Typical Output Characteristics
 $I_D=f(V_{DS}): 80\mu\text{s pulse test}, T_{ch}=25^\circ\text{C}$



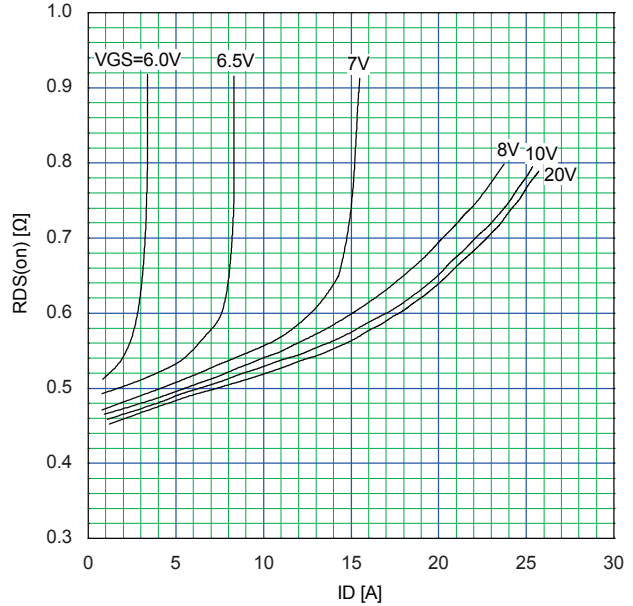
Typical Transfer Characteristic
 $I_D=f(V_{GS}): 80\mu\text{s pulse test}, V_{DS}=25\text{V}, T_{ch}=25^\circ\text{C}$



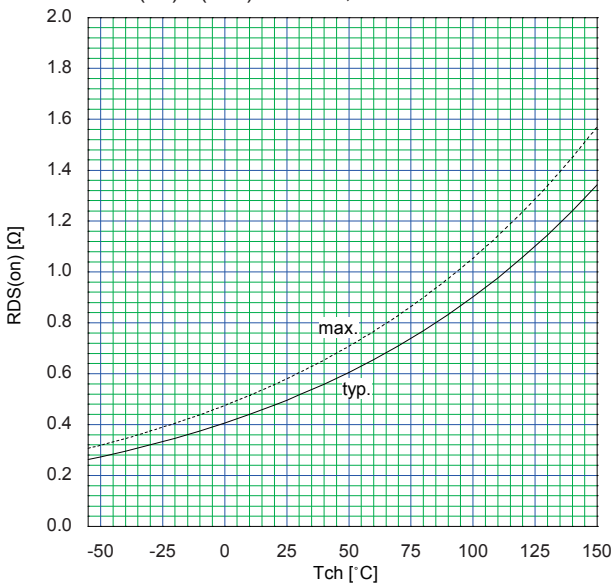
Typical Transconductance
 $g_{fs}=f(I_D): 80\mu\text{s pulse test}, V_{DS}=25\text{V}, T_{ch}=25^\circ\text{C}$



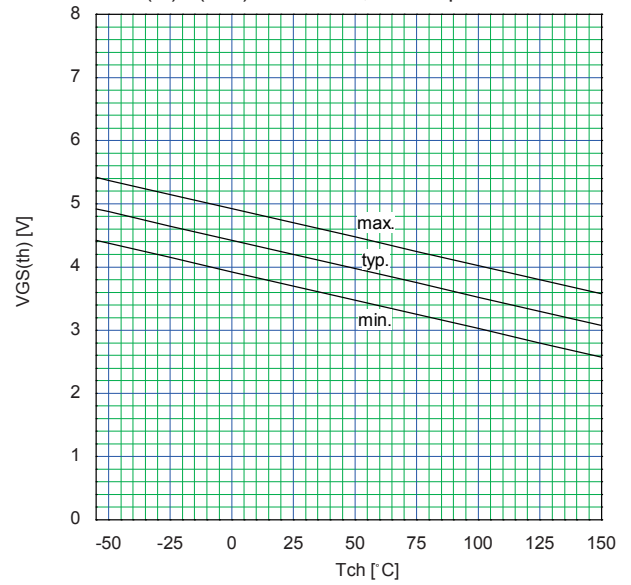
Typical Drain-Source on-state Resistance
 $R_{DS(on)}=f(I_D): 80\mu\text{s pulse test}, T_{ch}=25^\circ\text{C}$



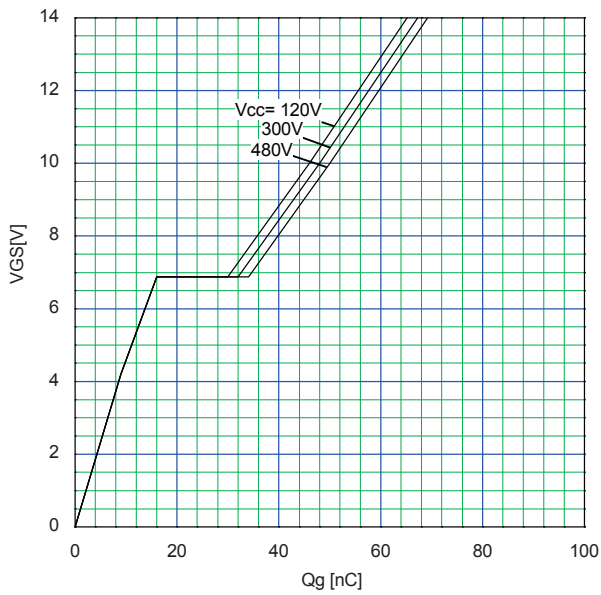
Drain-Source On-state Resistance
 $R_{DS(on)}=f(T_{ch}):I_D=6.5A, V_{GS}=10V$



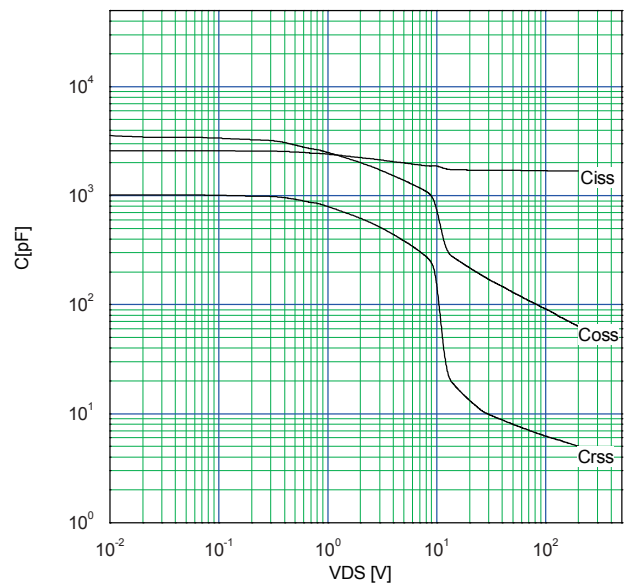
Gate Threshold Voltage vs. T_{ch}
 $V_{GS(th)}=f(T_{ch}):V_{DS}=V_{GS}, I_D=250\mu A$



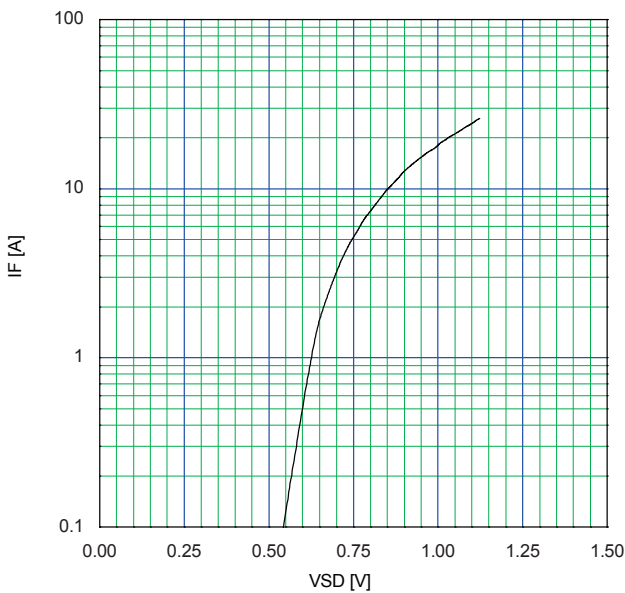
Typical Gate Charge Characteristics
 $V_{GS}=f(Q_g):I_D=13A, T_{ch}=25^\circ C$



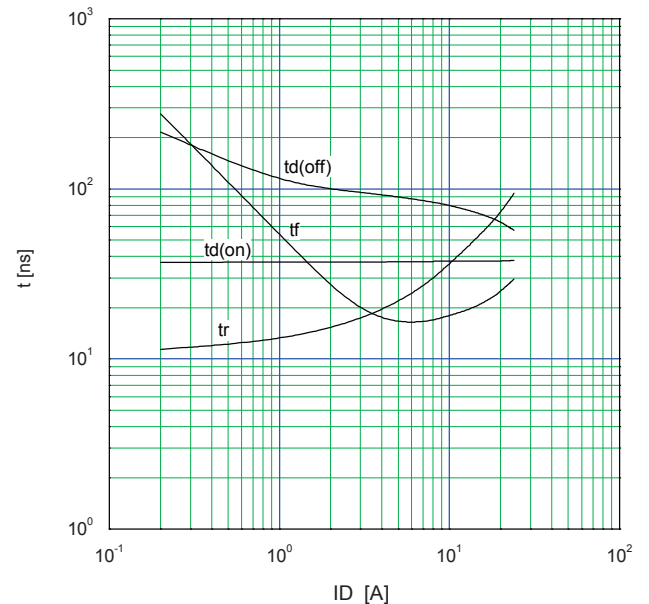
Typical Capacitance
 $C=f(V_{DS}):V_{GS}=0V, f=1MHz$



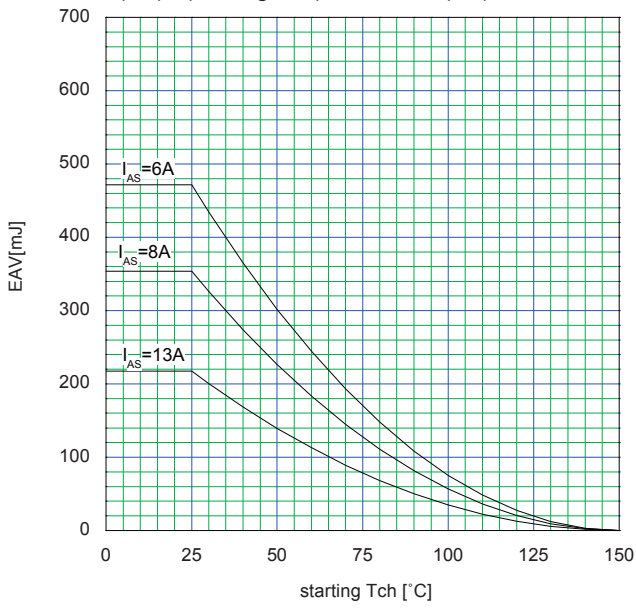
Typical Forward Characteristics of Reverse Diode
 $I_F=f(V_{SD}):80\mu s \text{ pulse test}, T_{ch}=25^\circ C$



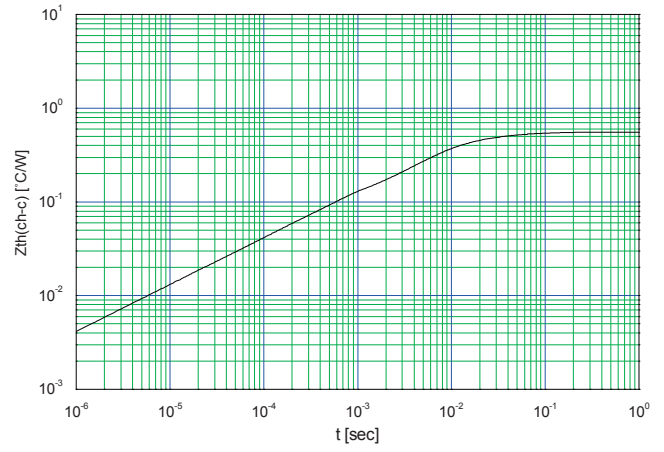
Typical Switching Characteristics vs. ID
 $t=f(I_D):V_{cc}=300V, V_{GS}=10V, R_G=18\Omega$



Maximum Avalanche Energy vs. starting Tch
 $E(AV)=f(\text{starting Tch}):V_{CC}=60V, I(AV)\leq 13A$



Maximum Transient Thermal Impedance
 $Z_{th(ch-c)}=f(t):D=0$



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